UC15&UC20

Compatible Design

UMTS/HSDPA Module Series

Rev. UC15&UC20_Compatible_Design_V1.2

Date: 2014-10-31

Our aim is to provide customers with timely and comprehensive service. For any assistance, please contact our company headquarters:

Quectel Wireless Solutions Co., Ltd.
Office 501, Building 13, No.99, Tianzhou Road, Shanghai, China, 200233
Tel: +86 21 5108 6236
Mail: info@quectel.com

Or our local office, for more information, please visit:
http://www.quectel.com/support/salesupport.aspx

For technical support, to report documentation errors, please visit:
http://www.quectel.com/support/techsupport.aspx

GENERAL NOTES

QUECTEL OFFERS THIS INFORMATION AS A SERVICE TO ITS CUSTOMERS. THE INFORMATION PROVIDED IS BASED UPON CUSTOMERS' REQUIREMENTS. QUECTEL MAKES EVERY EFFORT TO ENSURE THE QUALITY OF THE INFORMATION IT MAKES AVAILABLE. QUECTEL DOES NOT MAKE ANY WARRANTY AS TO THE INFORMATION CONTAINED HEREIN, AND DOES NOT ACCEPT ANY LIABILITY FOR ANY INJURY, LOSS OR DAMAGE OF ANY KIND INCURRED BY USE OF OR RELIANCE UPON THE INFORMATION. ALL INFORMATION SUPPLIED HEREIN IS SUBJECT TO CHANGE WITHOUT PRIOR NOTICE.

COPYRIGHT

About the Document

History

Revision	Date	Author	Description
1.0	2013-11-25	Mountain ZHOU	Initial
1.1	2014-02-13	Huik LI	1. Modified the frequency bands of UC15-A and UC20-A. 2. Modified description of I2C in Table 5.
1.2	2014-10-31	Huik LI	1. Released UC15 PCM function. 2. Updated recommended footprint in Figure 3. 3. Updated reference circuit of power supply in Figure 14. 4. Changed TXB0108PWR to TXS0108E in Figure 12. 5. Modified the frequency bands of UC15-A.

Contents

Table Index

Figure Index

1 Introduction

UC15 module is compatible with UC20 module. This document briefly describes the compatible design of UC15 and UC20. UC15 and UC20 can substitute each other in your design and manufacturing.

2 General Descriptions

2.1. Product Description

The UC15 is a UMTS/HSDPA module including two series, UC15-A and UC15-E, and UC20 is a UMTS/HSPA+ module including three series, UC20-A, UC20-E and UC20-G. The following tables show the frequency bands and module general information.

Table 1: Module Frequency Bands

Module	Frequency Bands
UC15-A	GSM850/900/1800/1900, UMTS850/1900
UC15-E	GSM900/1800, UMTS900/2100
UC20-A	UMTS850/1900
UC20-E	GSM850/900/1800/1900, UMTS900/2100
UC20-G	GSM850/900/1800/1900, UMTS800/850/900/1900/2100

Table 2: Module General Information

Module Name	Appearance	Packaging	Dimensions	Description
UC15		68-pin LCC+40 other pads	29 x 29 x 2.5mm	UMTS/HSDPA module (UC15-A and UC15-E)
UC20		72-pin LCC+40 other pads	29 x 32 x 2.5mm	UMTS/HSPA+ module (UC20-A, UC20-E and UC20-G)

UC15 and UC20 are designed as compatible products. You can choose the right module for your applications. Under the help of the compatible design guideline, you can migrate your products from UC20 to UC15 module smoothly.

2.2. Pin Assignment

The following figure shows the pin assignment of UC15 and UC20.

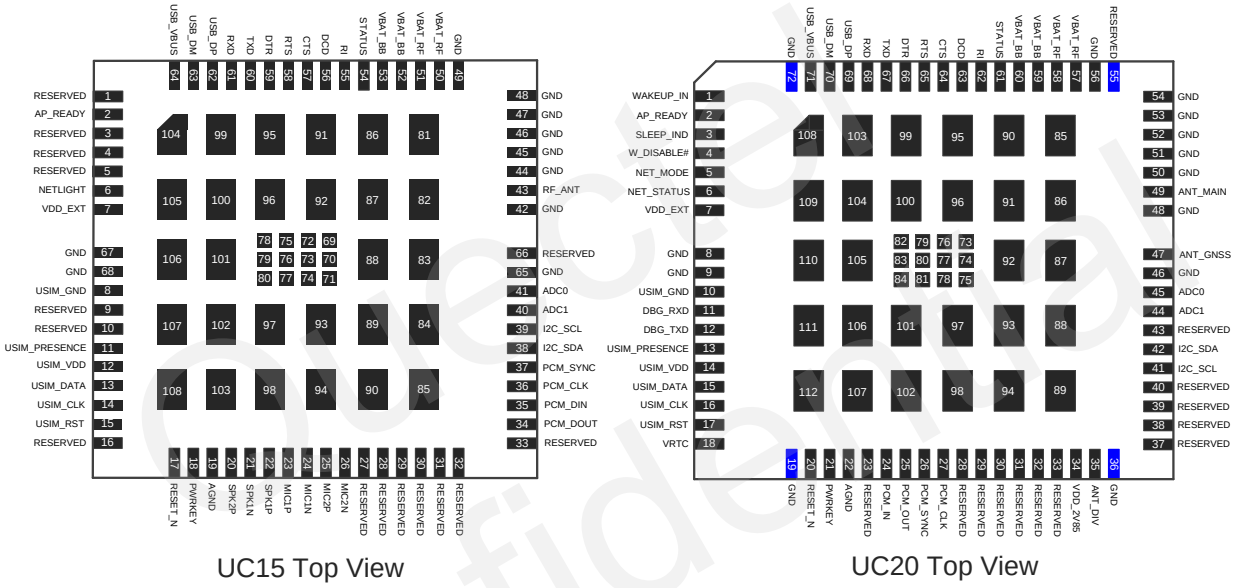

Figure 1: UC15&UC20 Pin Assignment

NOTE

The blue pins of UC20 are the additional pins compared with UC15.

Figure 2 shows the combination of pin assignment of UC15 and UC20.

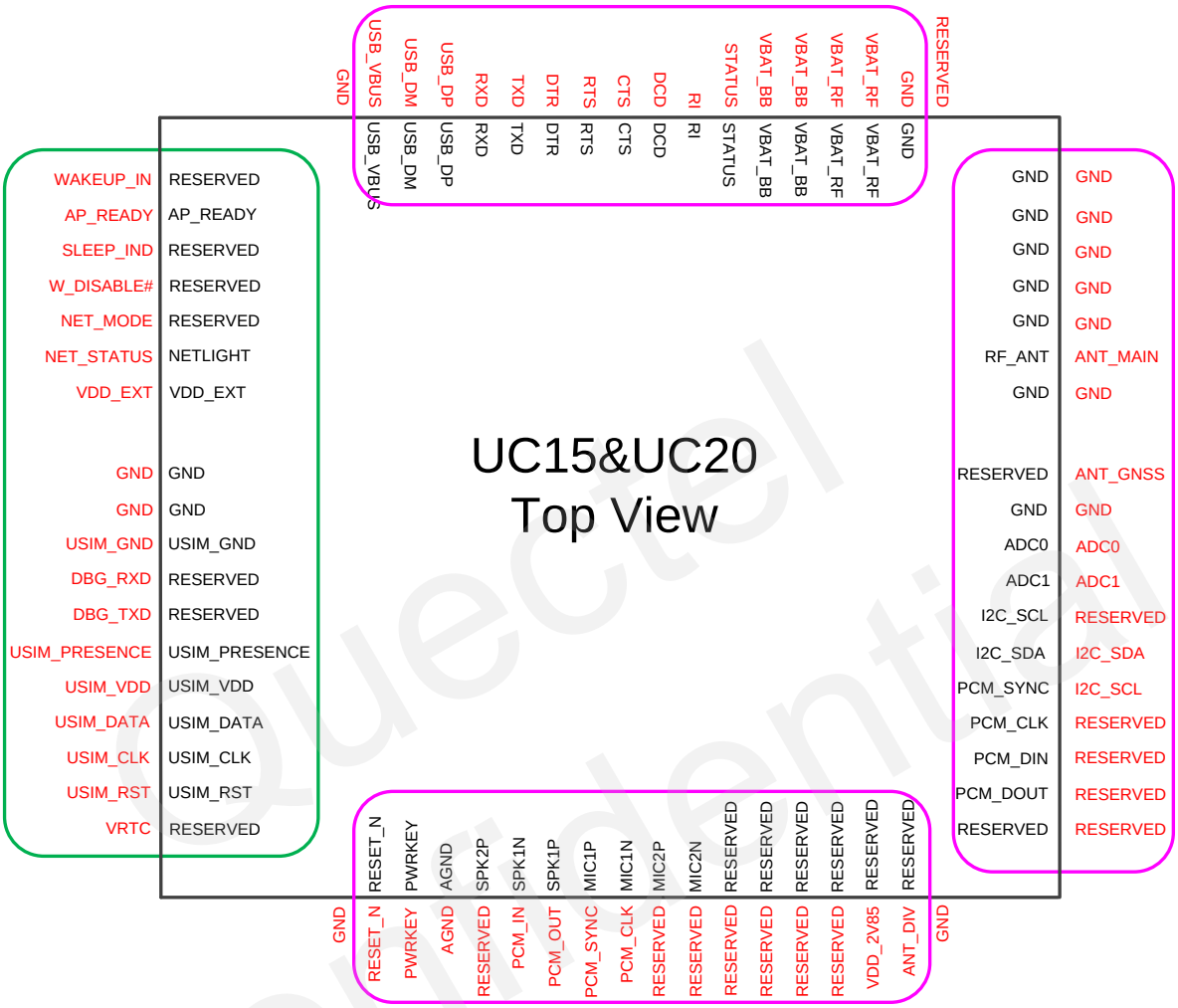

Figure 2: Combined Pin Assignment of UC15&UC20

NOTES

1. The pin names marked in red in the outside area are UC20's.
2. The pins in pink pane are compatible pins of UC15 and UC20 in same physical structure.
3. The pins in green pane are compatible pins of UC15 and UC20 on main functionality but different located structure. Pay attention to the recommended footprint and reference design of the compatibility when you design your applications.

3 Pin Description

This chapter describes the pin definition and assignment of UC15 and UC20.

Table 3: Parameters

Symbol	Description
IO	Bidirectional Input/output
DI	Digital Input
DO	Digital Output
PI	Power Input
PO	Power Output
AI	Analog Input
AO	Analog Output
OD	Open Drain

3.1. Common Pins

The following table shows common pins with the same function of UC15 and UC20.

Table 4: Common Pins

UC15				UC20			
Pin NO.	Pin Name	IO	Power Domain	Pin NO.	Pin Name	IO	Power Domain
2	AP_READY	DI	2.6V	2	AP_READY	DI	1.8V
6	NETLIGHT	DO	2.6V	6	NET_STATUS	DO	1.8V
7	VDD_EXT	PO	2.6V	7	VDD_EXT	PO	1.8V

67	GND	-	Ground	8	GND	-	Ground
68	GND	-	Ground	9	GND	-	Ground
8	USIM_GND	-	Ground	10	USIM_GND	-	Ground
11	USIM_PRESENCE	DI	2.6V	13	USIM_PRESENCE	DI	1.8V
12	USIM_VDD	PO	1.8/3.0V	14	USIM_VDD	PO	1.8/3.0V
13	USIM_DATA	IO	1.8/3.0V	15	USIM_DATA	IO	1.8/3.0V
14	USIM_CLK	DO	1.8/3.0V	16	USIM_CLK	DO	1.8/3.0V
15	USIM_RST	DO	1.8/3.0V	17	USIM_RST	DO	1.8/3.0V
17	RESET_N	DI	1.8V	20	RESET_N	DI	1.8V
18	PWRKEY	DI	1.8V	21	PWRKEY	DI	1.8V
19	AGND	-	Ground	22	AGND	-	Ground
27	RESERVED	-	-	30	RESERVED	-	-
28	RESERVED	-	-	31	RESERVED	-	-
29	RESERVED	-	-	32	RESERVED	-	-
30	RESERVED	-	-	33	RESERVED	-	-
33	RESERVED	-	-	37	RESERVED	-	-
40	ADC1	AI	0~2.1V	44	ADC1	AI	0.2~4.2V
41	ADC0	AI	0~2.1V	45	ADC0	AI	0.2~2.1V
65	GND	-	Ground	46	GND	-	Ground
42	GND	-	Ground	48	GND	-	Ground
43	RF_ANT	IO	-	49	ANT_MAIN	IO	-
44	GND	-	Ground	50	GND	-	Ground
45	GND	-	Ground	51	GND	-	Ground
46	GND	-	Ground	52	GND	-	Ground
47	GND	-	Ground	53	GND	-	Ground
48	GND	-	Ground	54	GND	-	Ground

49	GND	-	Ground	56	GND	-	Ground
50	VBAT_RF	PI	3.3~4.3V	57	VBAT_RF	PI	3.3~4.3V
51	VBAT_RF	PI	3.3~4.3V	58	VBAT_RF	PI	3.3~4.3V
52	VBAT_BB	PI	3.3~4.3V	59	VBAT_BB	PI	3.3~4.3V
53	VBAT_BB	PI	3.3~4.3V	60	VBAT_BB	PI	3.3~4.3V
54	STATUS	DO	2.6V	61	STATUS	OD	-
55	RI	DO	2.6V	62	RI	DO	1.8V
56	DCD	DO	2.6V	63	DCD	DO	1.8V
57	CTS	DO	2.6V	64	CTS	DO	1.8V
58	RTS	DI	2.6V	65	RTS	DI	1.8V
59	DTR	DI	2.6V	66	DTR	DI	1.8V
60	TXD	DO	2.6V	67	TXD	DO	1.8V
61	RXD	DI	2.6V	68	RXD	DI	1.8V
62	USB_DP	IO	-	69	USB_DP	IO	-
63	USB_DM	IO	-	70	USB_DM	IO	-
64	USB_VBUS	PI	Typ.5V	71	USB_VBUS	PI	Typ.5V
69~80	RESERVED	-	-	73~84	RESERVED	-	-
81~108	GND	-	-	85~112	GND	-	-

3.2. Different Functional Pins

The following table shows the different functional pins of UC15 compared with UC20.

Table 5: Different Functional Pins

UC15				UC20			
Pin NO.	**Pin Name**	**IO**	**Power Domain**	**Pin NO.**	**Pin Name**	**IO**	**Power Domain**

1	RESERVED	-	-	1	WAKEUP_IN	I	1.8V
3	RESERVED	-	-	3	SLEEP_IND	DO	1.8V
4	RESERVED	-	-	4	W_DISABLE#	DI	1.8V
5	RESERVED	-	-	5	NET_MODE	DO	1.8V
9	RESERVED	-	-	11	DBG_RXD	DI	1.8V
10	RESERVED	-	-	12	DBG_TXD	DO	1.8V
16	RESERVED	-	-	18	VRTC	IO	1.5~3.25V
-	-	-	-	19	GND	-	-
20	SPK2P	AO	-	23	RESERVED	-	-
21	SPK1N	AO	-	24	PCM_IN	DI	1.8V
22	SPK1P	AO	-	25	PCM_OUT	DO	1.8V
23	MIC1P	AI	-	26	PCM_SYNC	IO	1.8V
24	MIC1N	AI	-	27	PCM_CLK	IO	1.8V
25	MIC2P	AI	-	28	RESERVED	-	-
26	MIC2N	AI	-	29	RESERVED	-	-
31	RESERVED	-	-	34	VDD_2V85	PO	2.85V
32	RESERVED	-	-	35	ANT_DIV	AI	-
-	-	-	-	36	GND	-	-
34	PCM_DOUT	DO	2.6V	38	RESERVED	-	-
35	PCM_DIN	DI	2.6V	39	RESERVED	-	-
36	PCM_CLK	IO	2.6V	40	RESERVED	-	-
37	PCM_SYNC	IO	2.6V	41	I2C_SCL	OD	1.8V
38	I2C_SDA	IO	2.6V	42	I2C_SDA	OD	1.8V
39	I2C_SCL	DO	2.6V	43	RESERVED	-	-
66	RESERVED	-	-	47	ANT_GNSS	AI	
-	-	-	-	55	RESERVED	-	-

-	-	-	-	72	GND	-	-

NOTES

1. Keep all reserved and unused pins unconnected.
2. For different functional pins, if necessary, please reserve 0 ohm resistors.
3. All GND pins should be connected to ground.

4 Recommended Footprint

The following figure shows the recommended compatible footprint of UC15 and UC20.

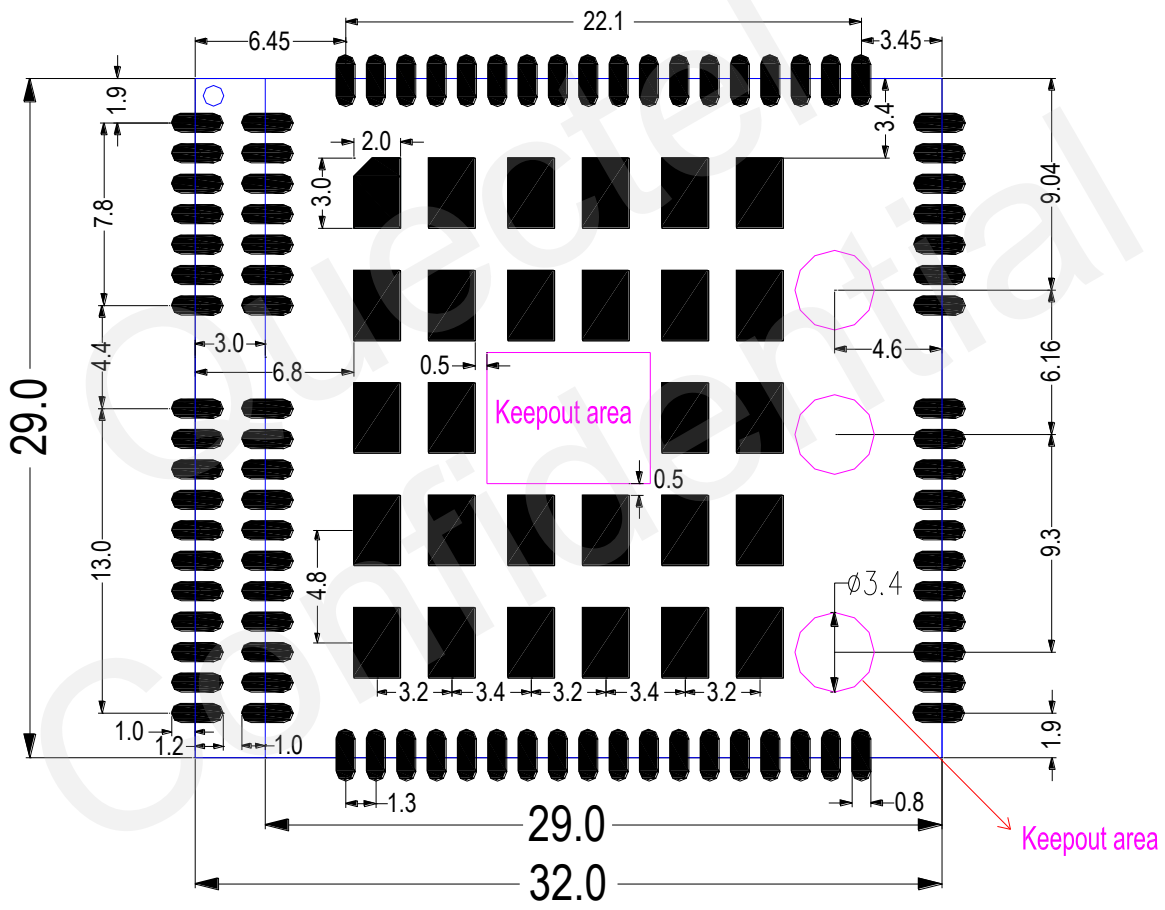

Figure 3: Recommended Footprint (Unit: mm)

NOTES

1. The areas in three circles should be kept out.
2. The area in the rectangle are the pins 69~80 of UC15 or pins 73~84 of UC20 used for factory test. It

is recommended to keep this area out in PCB decal.

The following figure shows the sketch map of installation between UC15 and UC20.

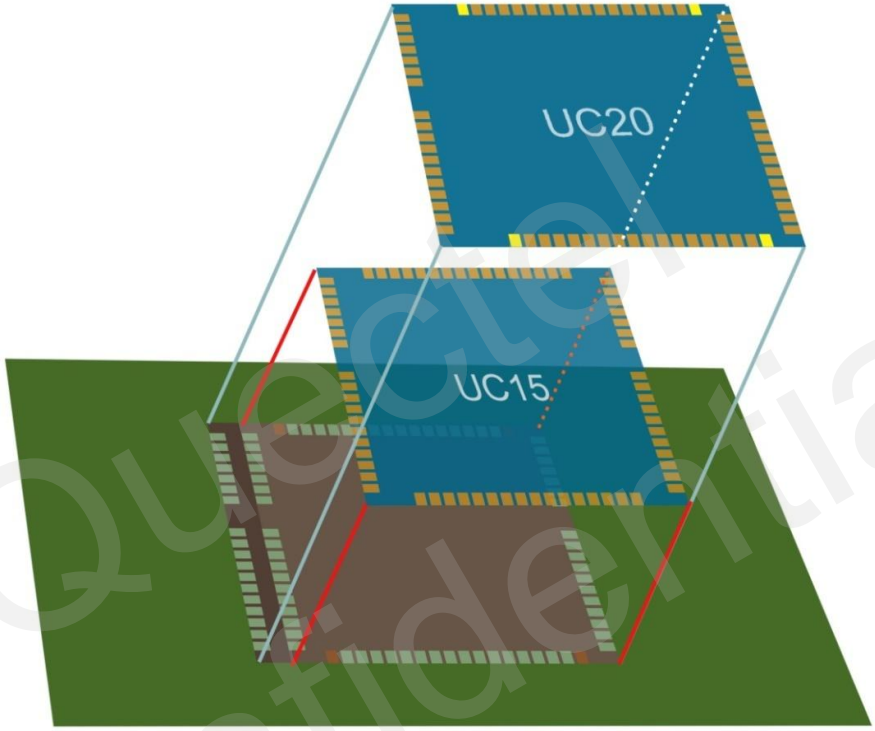

Figure 4: Renderings of Installation

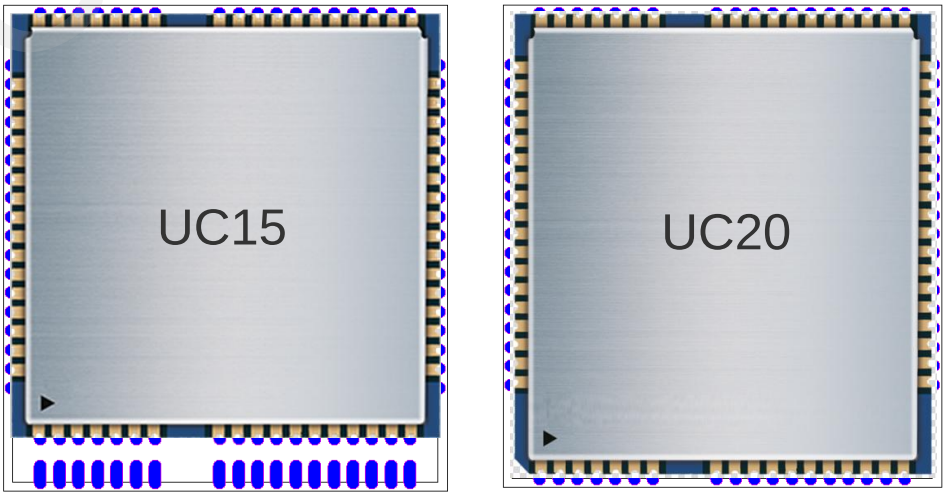

Figure 5: Actual Installation

5 Hardware Reference Design

The following chapters describe compatible design of UC15 and UC20 on main functionalities.

5.1. Power on Circuit

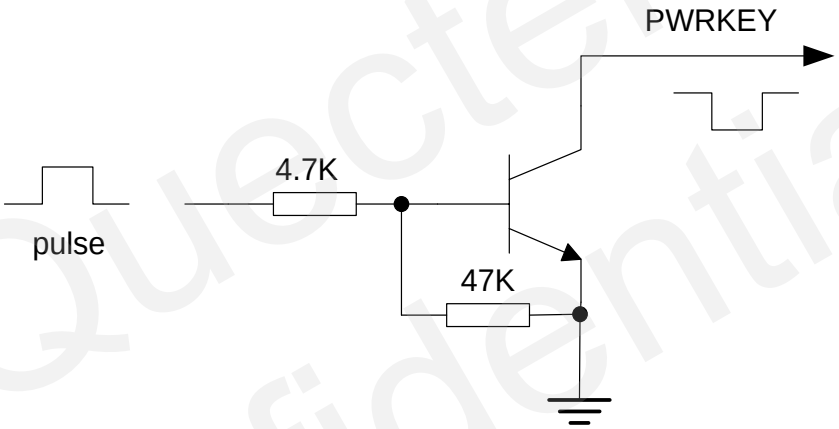

Figure 6: Turn on the Module Using Driving Circuit

5.2. RESET Circuit

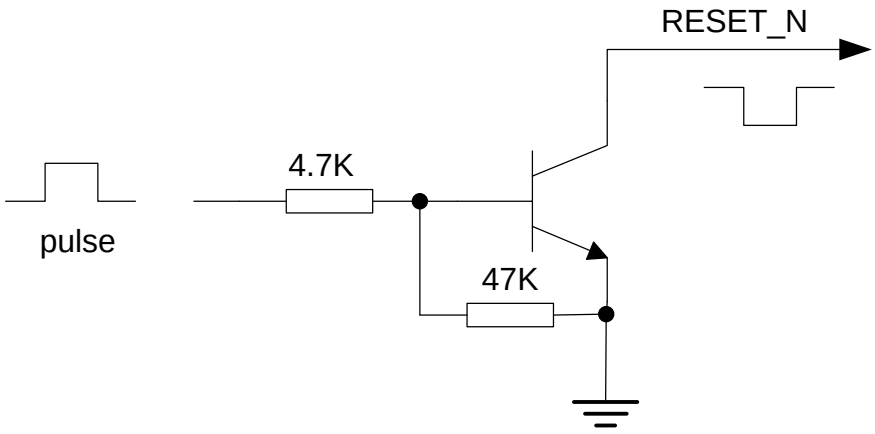

Figure 7: Driving Circuit of Resetting the Module

NOTE

As to UC15, the pulse time of reset must be between 50ms and 200ms, otherwise the module will be powered off.

5.3. Network Status Indication

The NETLIGHT (the NET_STATUS on UC20) signal can be used to drive a network status indicator LED. The following circuit is the reference design of NETLIGHT.

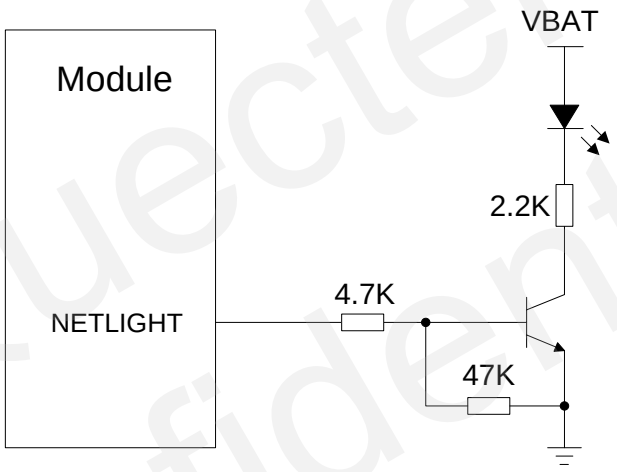

Figure 8: Reference Circuit of the NETLIGHT

5.4. Operating Status Indication

STATUS outputs high level after module is turned on successfully. UC15's STATUS is a GPO pin, while UC20's STATUS is an open-drain output. The following figures show the reference circuits of driving LED for UC15 and UC20 modules.

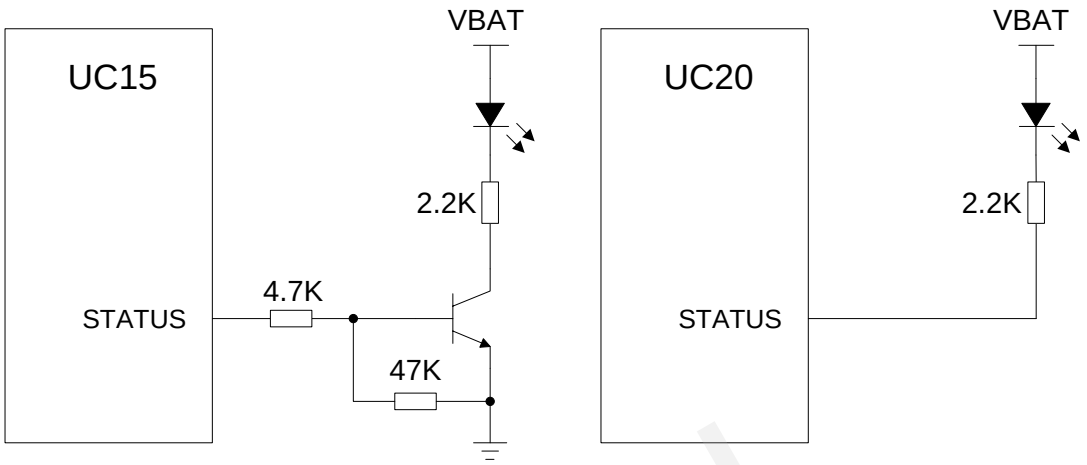

Figure 9: Reference Circuit of the STATUS

5.5. USB Interface

UC15 and UC20 contain one integrated Universal Serial Bus (USB) transceiver which complies with the USB 2.0 specification and supports high speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps) mode. The USB interfaces of UC15 and UC20 are primarily used for AT command, data transmission, software debugging and firmware upgrade. Besides, the USB interface of UC20 can be used as GNSS NMEA output. More details about the USB 2.0 specifications, please visit http://www.usb.org/home.

The following figure shows the reference circuit of USB interface.

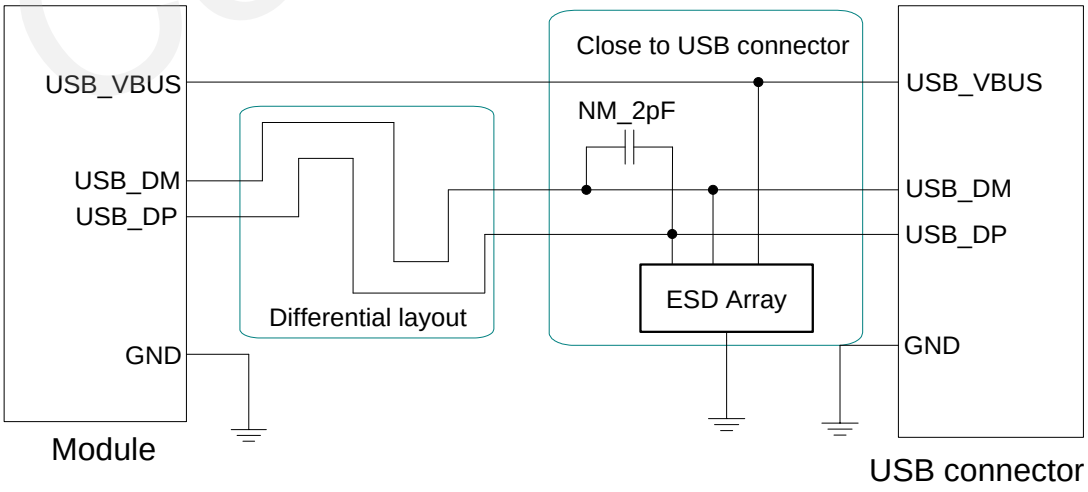

Figure 10: Reference Circuit of the USB Application

In order to ensure the USB interface design corresponding with the USB 2.0 specification, please do remember to comply with the following principles:

- Keep the ESD components as closer to the USB connector as possible.
- Pay attention to the influence of junction capacitance of ESD component on USB data lines. Typically, the capacitance value should be less than 2pF.
- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90ohm.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding not only upper and lower layer but also right and left side.

NOTE

UC15 and UC20 module can only be used as a USB slave device.

5.6. USIM Interface

USIM interfaces of UC15 and UC20 support 1.8V or 3.0V USIM cards automatically.

You can tie UC20's USIM pins to UC15's directly and then route to USIM card cassette. The following figure shows the USIM reference design with USIM card detection function.

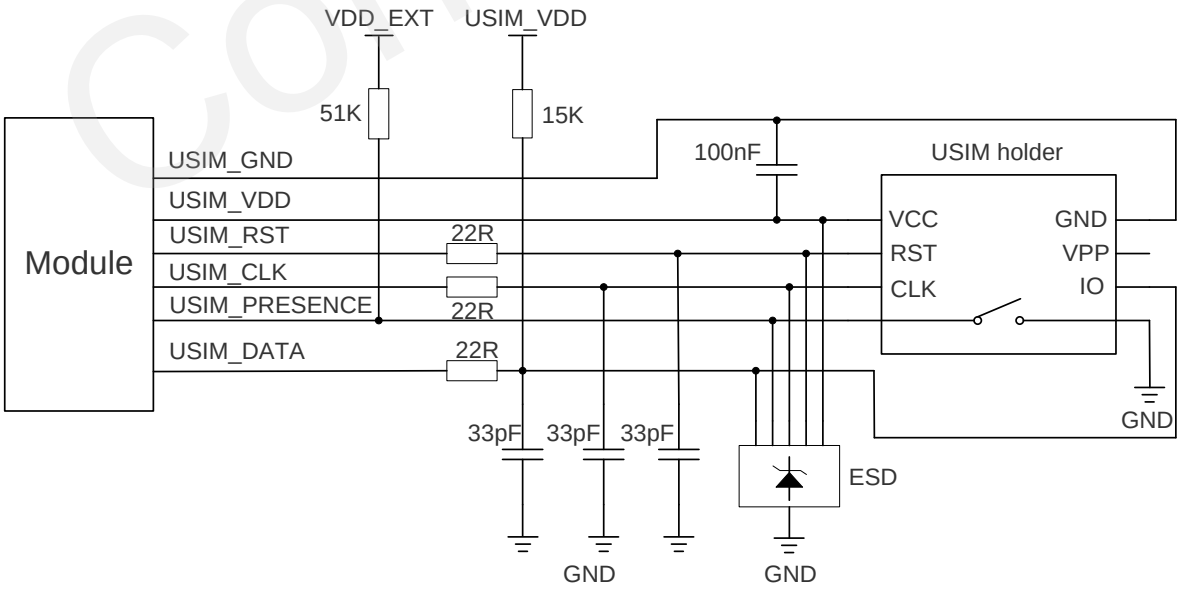

Figure 11: Reference Design of SIM Interface

5.7. UART Interface

Because of the different power domain of the UART interface, you need to add level match circuit between UC15 or UC20 module and MCU.

The following circuit shows reference design of UART interface level match.

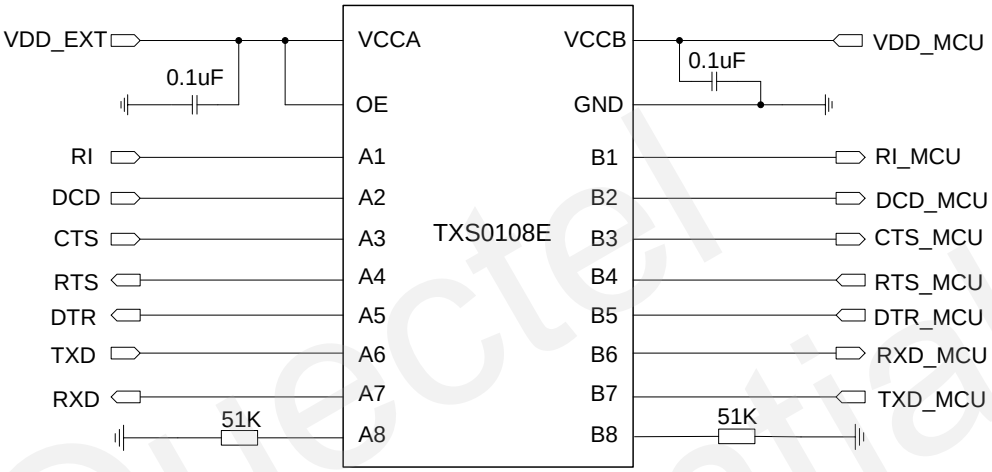

Figure 12: Reference Design of UART Interface

NOTES

1. UART pins of UC15 belong to 2.6V power domain.
2. UART pins of UC20 belong to 1.8V power domain.

5.8. ADC Interface

Both UC15 and UC20 have two ADC pins for general purpose analog-to-digital converter. UC15's ADC pins are compatible with UC20's. But there are some differences in their voltage range. The following table shows the differences between UC15 and UC20.

Table 6: ADC Voltage Range

Channel	UC15	UC20
ADC0	0~2.1V	0.2~2.1V
ADC1	0~2.1V	0.2~4.2V

5.9. RF Interface

The UC15 pin 43 (UC20 pin 49) is the RF antenna pad. The RF interface has an impedance of 50Ω. A reference circuit is shown in the following figure. In order to adjust RF performance, it should reserve a π-type matching circuit. By default, the resistance of R1 is 0Ω and capacitors C1 and C2 are not mounted.

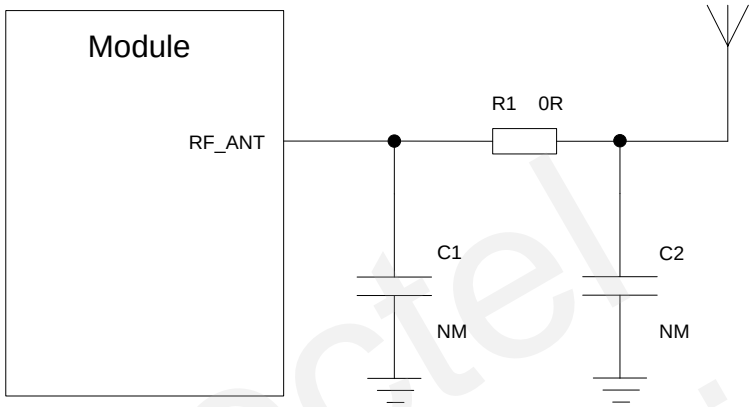

Figure 13: Reference Circuit of RF Interface

5.10. Power Supply

The power supply range of the UC15&UC20 is 3.3~4.3V. Attention should be paid in the range of the power source to make sure that the input voltage will never drop below 3.3V and never exceed 4.3V. The typical power supply of UC15 and UC20 is about 3.8V. The following figure shows a reference design for +5V input power source. The designed output for the power supply is about 3.8V and the maximum load current is 3A. The VBAT to VBAT_BB and VBAT_RF pins should be divided into two separated paths in star structure. In addition, in order to get a stable output voltage, it is suggested to use a zener diode whose reverse zener voltage is 5.1V and power dissipation is more than 0.5 watt.

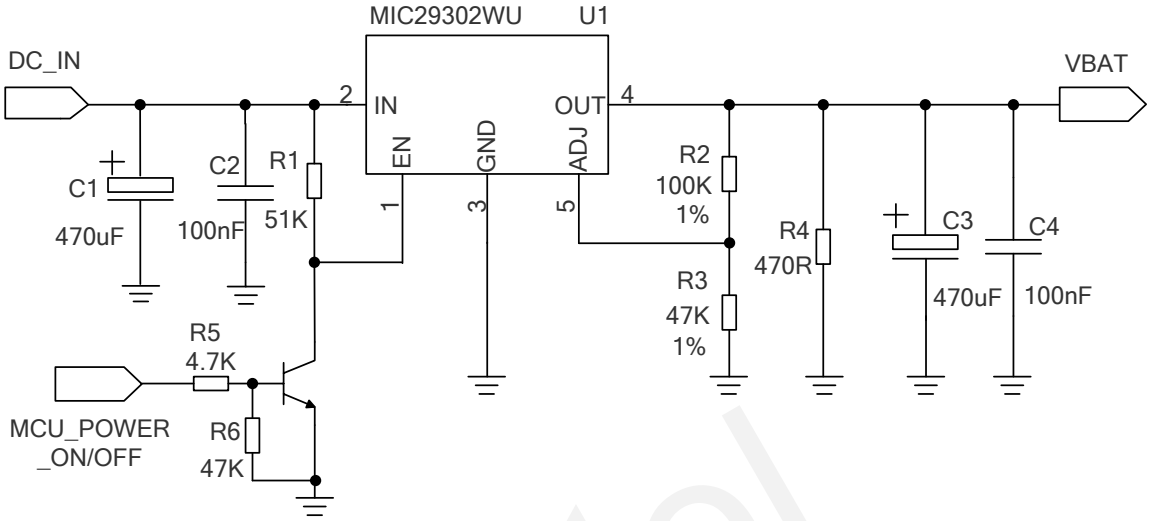

Figure 14: Reference Circuit of Power Supply

NOTE

When the module cannot be turned off by PWRKEY pin or in other abnormal status, it is suggested to switch off the power supply for module and power it on later.

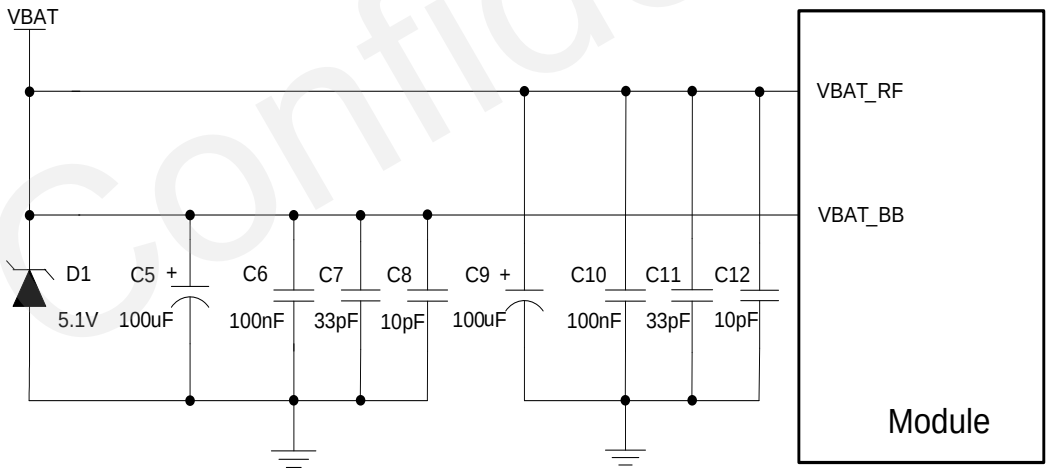

Figure 15: Reference Circuit of Star Structure

6 Appendix A

Table 7: Related Documents

SN	Document Name	Remark
[1]	UC15_Hardware_Design	UC15 Hardware Design
[2]	UC20_Hardware_Design	UC20 Hardware Design
[3]	UC15_Reference_Design	UC15 Reference Design
[4]	UC20_Reference_Design	UC20 Reference Design
[5]	UC15&UC20_Reference_Design	UC15&UC20 Reference Design