

Features

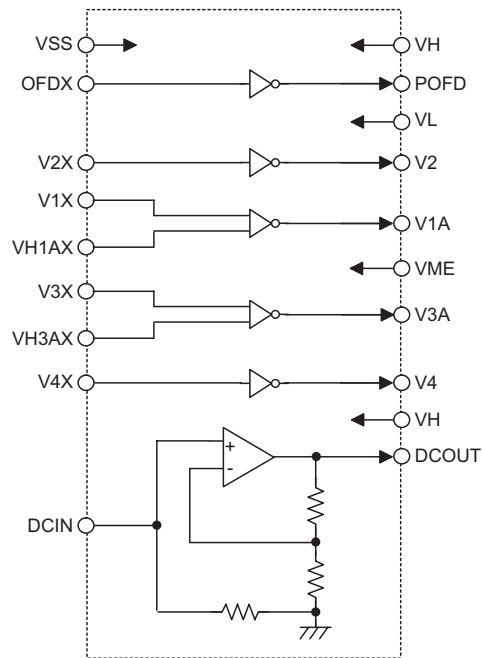
- Input voltage: 3.0V~5.5V
- Built-in seven circuits
 - 2-level output:
 - 2 circuits for vertical CCD clock driver
output voltage level (typ.) = -9V to 0V
 - 3-level output:
 - 2 circuits for vertical CCD clock driver
output voltage level (typ.) = -9V to 15V
 - 2-level output:
 - 1 circuit for shutter driver
output voltage level (typ.) = -9V to 15V
- Switchable between NTSC (EIA) and PAL (CCIR) modes
- 16-pin SSOP, 16/20-pin TSSOP package

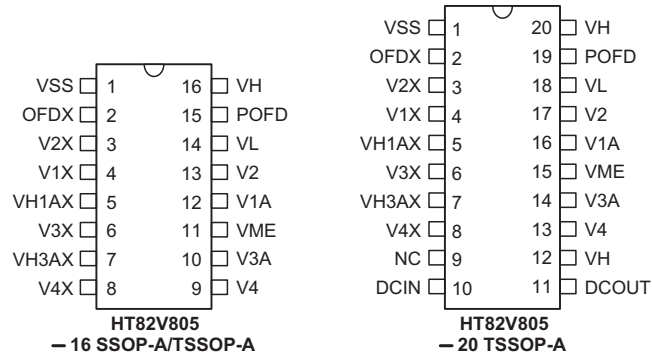
General Description

HT82V805 is a CMOS vertical clock driver and shutter driver IC for CCD area sensors. It has the capability of

converting the voltage and impedance from the CMOS level.

Block Diagram



Pin Assignment

Pin Description

Pin Name	I/O	Description
VSS	—	Negative power supply, ground
OFDX	I	Electronic shutter pulse input
V1X, V2X, V3X, V4X	I	Vertical transfer pulse input
VH1AX, VH3AX	I	Pulse that transfers the charge of the photo-diode to the vertical shift register.
NC	—	No connection
DCIN	I	OP-Amp input (internal pull-down resistor)
DCOUT	O	OP-Amp output
VH	—	Power supply for high level of V1A, V3A
V4	O	Pulse to drive vertical CCD shift register (2 level: VME, VL)
V3A	O	Pulse to drive vertical CCD shift register (3 level: VME, VL, VH)
VME	—	Power supply for intermediate level of V1A, V3A
V1A	O	Pulse to drive vertical CCD shift register (3 level: VME, VL, VH)
V2	O	Pulse to drive vertical CCD shift register (2 level: VME, VL)
VL	—	Power supply for all low level output pulses
POFD	O	Electronic shutter pulse output (2 level: VL, VH)

Absolute Maximum Ratings

Supply Voltage $V_{SS}-0.3V$ to V_L+35V Storage Temperature $-55^{\circ}C$ to $150^{\circ}C$
 Input Voltage $V_{SS}-0.3V$ to $V_H+0.3V$ Operating Temperature $-25^{\circ}C$ to $70^{\circ}C$

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_H	Supply Voltage	$-0.3 \sim V_L+35$	V
V_L		$0 \sim -10$	V
VME		$V_L-0.3 \sim 3.0$	V
V1A, V2, V3A, V4, POFD	Output Voltage	$V_L-0.3 \sim V_H+0.3$	V

Logic Function Table

Input				Output		
V1X, V3X	VH1AX, VH3AX	V2X, V4X	OFDX	V1A, V3A	V2, V4	POFD
L	L	—	—	VH	—	—
H	L	—	—	Z	—	—
L	H	—	—	VME	—	—
H	H	—	—	VL	—	—
—	—	L	—	—	VME	—
—	—	H	—	—	VL	—
—	—	—	L	—	—	VH
—	—	—	H	—	—	VL

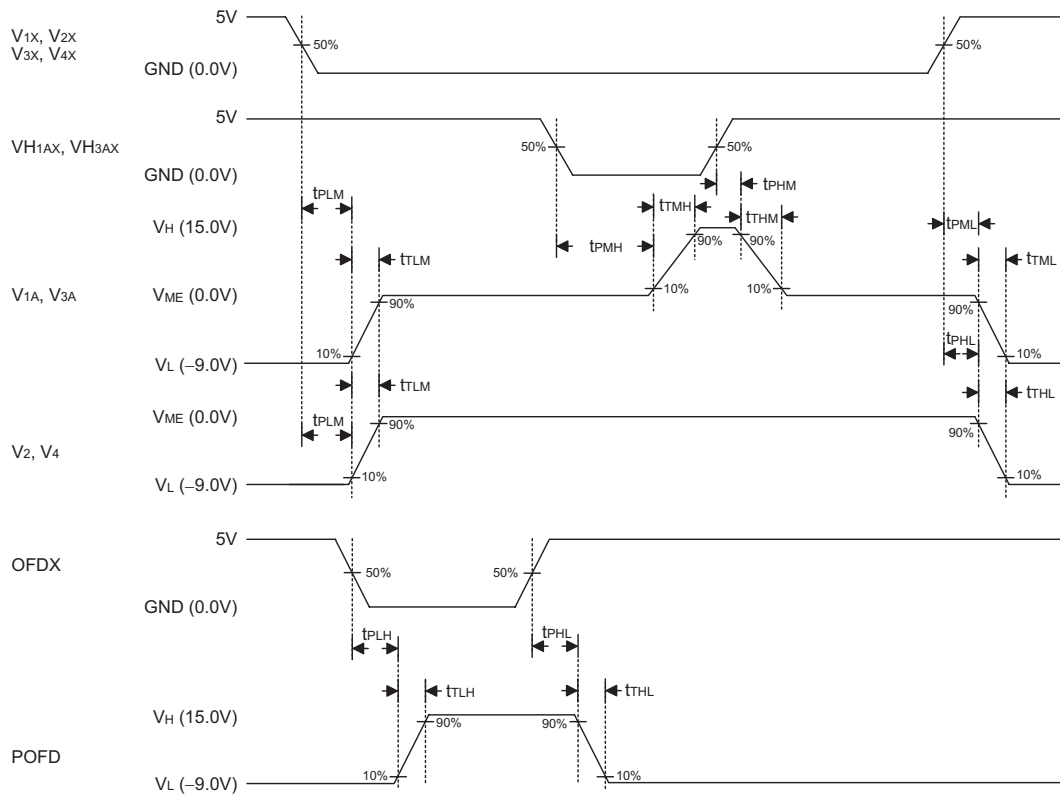
D.C. Characteristics
 $V_H=15V, V_L=-9V, V_{ME}=0V, T_a=25^\circ C$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Logic Supply Voltage	—	3.0	3.3	5.5	V
V_H	Supply Voltage	—	14.5	15	15.5	V
V_L	Supply Voltage	—	-9.5	-8.5	-7.5	V
V_{IH}	High Level Input Voltage	—	2.4	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	1.2	V
I_{VH}	Operating Current	Shutter speed=100kHz	—	3.8	—	mA
I_{VL}			—	-2	—	mA
I_{VME}			—	-6.5	—	mA
I_{OL}	Output Current	$V_{1A}, V_2, V_{3A}, V_4=-9.0V$	—	37	—	mA
I_{OM1}		$V_{1A}, V_2, V_{3A}, V_4=-0.5V$	—	-15	—	mA
I_{OM2}		$V_{1A}, V_{3A}=0.5V$	—	13.5	—	mA
I_{OH}		$V_{1A}, V_{3A}=14.5V$	—	-18	—	mA
I_{OSL}		$O_{FDX}=-8.0V$	—	18	—	mA
I_{OSH}		$O_{FDX}=14.5V$	—	-10.5	—	mA
G		OP-Amp Gain	$DCIN=1\sim 3V$	3.4	3.9	4.2

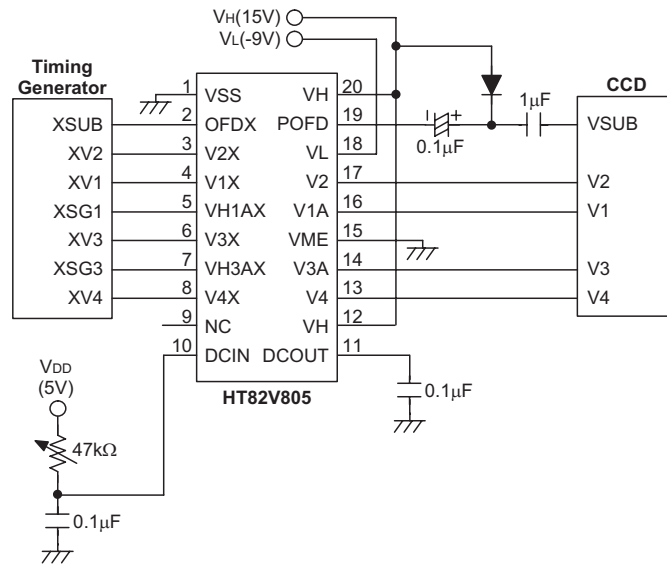
A.C. Characteristics
 $T_a=25^\circ C$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLM}	Delay Time	$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	55	80	ns
t_{PMH}		$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	50	90	ns
t_{PLH}		$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	55	100	ns
t_{PML}		$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	45	130	ns
t_{PHM}		$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	50	120	ns
t_{PHL}		$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	55	100	ns
t_{TLM}	Rising Time	$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	370	900	ns
t_{TMH}		$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	785	900	ns
t_{TLH}		$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	70	140	ns
t_{TML}		$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	300	700	ns
t_{THM}		$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	630	960	ns
t_{THL}		$V_H=15V, V_L=-8.5V, V_{ME}=0V$	—	45	120	ns

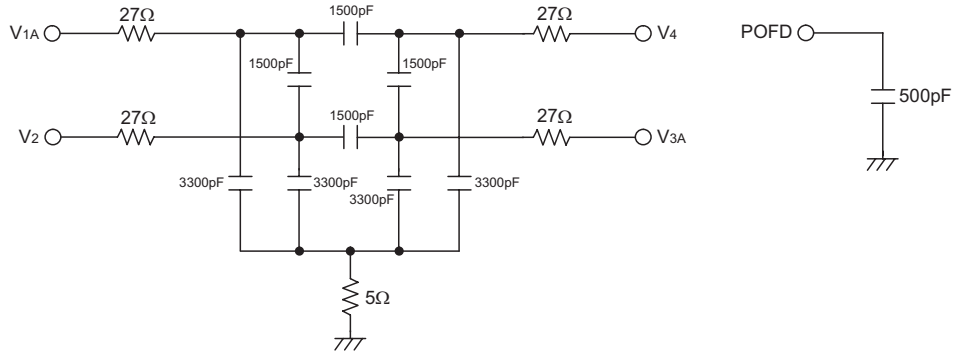
Timing Diagrams



Application Circuits

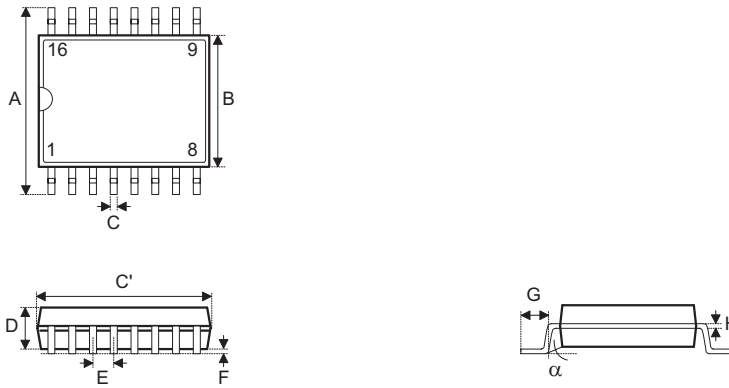


Equivalent Circuits



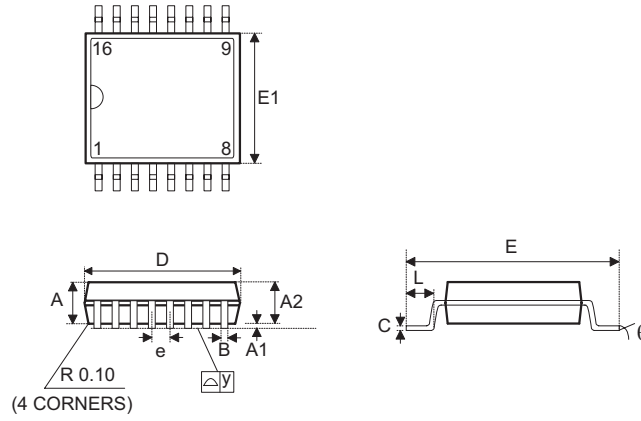
Package Information

16-pin SSOP (150mil) Outline Dimensions



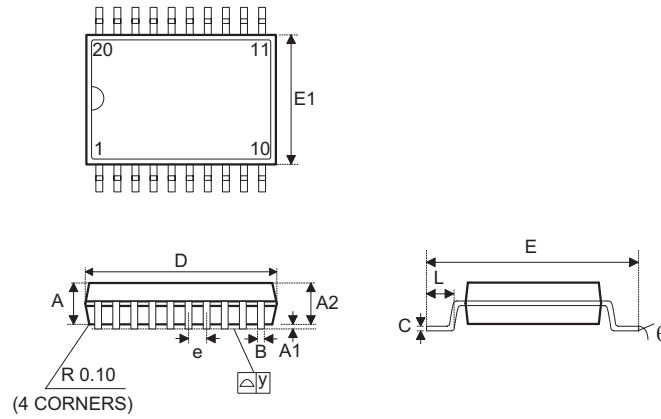
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	150	—	157
C	8	—	12
C'	189	—	197
D	54	—	60
E	—	25	—
F	4	—	10
G	22	—	28
H	7	—	10
α	0°	—	8°

16-pin TSSOP Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	1	—	1.05
A1	0.05	—	0.15
A2	1.05	—	1.2
B	—	0.25	—
C	0.11	—	0.15
D	4.9	—	5.1
E	6.2	—	6.6
E1	4.3	—	4.5
e	—	0.65	—
L	0.5	—	0.7
y	—	—	0.076
θ	0°	—	8°

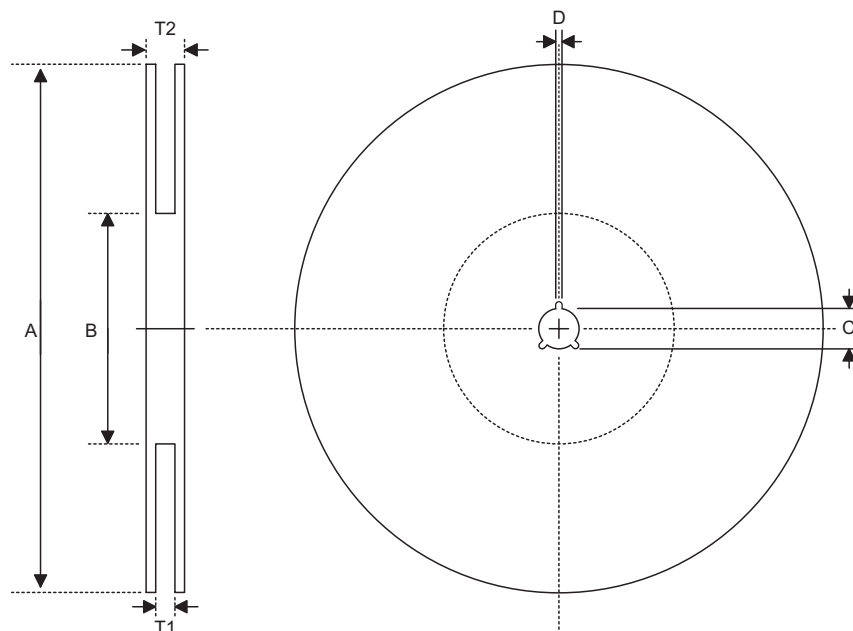
20-pin TSSOP Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	1.05	—	1.2
A1	0.05	—	0.15
A2	0.95	—	1.05
B	—	0.22	—
C	0.13	—	0.17
D	6.4	—	6.6
E	6.3	—	6.5
E1	4.3	—	4.5
e	—	0.65	—
L	0.45	—	0.75
y	—	—	0.1
θ	0°	—	8°

Product Tape and Reel Specifications

Reel Dimensions



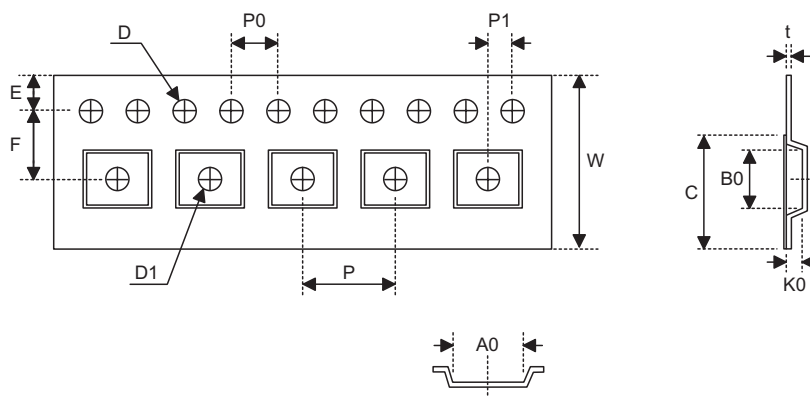
SSOP 16S

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13.0+0.5 -0.2
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	12.8+0.3 -0.2
T2	Reel Thickness	18.2±0.2

TSSOP 16L

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13+0.5 -0.2
D	Key Slit Width	2±0.5
T1	Space Between Flange	16.8+0.3 -0.2
T2	Reel Thickness	22.2±0.2

Carrier Tape Dimensions



SSOP 16S

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0+0.3 -0.1
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.2±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	9.3

TSSOP 16L

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16+0.3 -0.1
P	Cavity Pitch	8±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	7.5±0.5
D	Perforation Diameter	1.5+0.1
D1	Cavity Hole Diameter	1.5+0.1
P0	Perforation Pitch	4±0.1
P1	Cavity to Perforation (Length Direction)	2±0.1
A0	Cavity Length	6.8±0.1
B0	Cavity Width	5.4±0.1
K0	Cavity Depth	1.6±0.1
t	Carrier Tape Thickness	0.3±0.013
C	Cover Tape Width	13.3

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