
MPLAB[®] ICE 2000 Processor Module Errata Sheet

For MPLAB ICE 2000 processor modules PCM18XA0 and PCM18XB0, the following operational issues should be noted:

- Initialization code for table reads needed
- I²C[™] Master Mode – Opcode xxC9 Execution Clears BF Bit

Please note that these are emulator-only issues. Operation of the actual device is not affected.

Initialization code for table reads needed

The following initialization code needs to be added to your firmware for proper Table Reads when using interrupts with the MPLAB ICE 2000 PCM18XA0/B0 Processor Module. This code snippet can be removed when you program an actual part.

If your firmware is in C, the following code needs to be added as the first instruction in `main()`, (i.e., your code should look like this):

```
void main(void)
{
    { _asm movlw 0xb0 movwf 0xf9c,0 _endasm }
```

If your firmware is in assembly, the following code needs to be added to the initialization code:

```
movlw 0xb0
movwf 0xf9c
```

0xf9c is a reserved location and you should not perform any other writes to 0xf9c in your code – a read at address 0xf9c will always return a zero. As a general precaution, do not read or write unused Special Function Registers.

If this code snippet is not executed in your code, you may experience extra cycles on Table Read instructions and faulty instruction execution on the instruction following a Table Read instruction, if an interrupt occurs when executing the Table Read.

I²C Master Mode – Opcode xxC9 Execution Clears BF Bit

For I²C Master Mode, an execution of any opcode of the form xxC9 (where x is any hexadecimal digit) will clear the SSPSTAT BF bit. That is, an execution of an xxC9 opcode will cause SSPBUF to be read, thus clearing the SSPSTAT bit BF.

Many opcodes can be encoded as xxC9, such as GOTO, Branches, ANDLW, etc. These instructions will clear the BF bit in the emulator only. The actual PIC18Cxxx micro will function properly.

NOTES:

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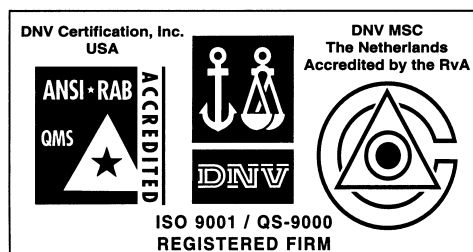
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WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
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Tel: 480-792-7200 Fax: 480-792-7277
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Web Address: <http://www.microchip.com>

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Dallas

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Addison, TX 75001
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Dayton

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Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit

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32255 Northwestern Highway, Suite 190
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Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles

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Mountain View

Analog Product Sales
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Mountain View, CA 94043-1836
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New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Beijing Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Shanghai

Microchip Technology Shanghai Office
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

Hong Kong

Microchip Asia Pacific
RM 2101, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

ASIA/PACIFIC (continued)

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Denmark ApS
Regus Business Centre
Lautrup hof 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Germany

Analog Product Sales
Lochamer Strasse 13
D-82152 Martinsried, Germany
Tel: 49-89-895650-0 Fax: 49-89-895650-22

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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