MICROCHIP PIC16C63A/65B/73B/74B

PIC16C63A/65B/73B/74B Rev. A Silicon/Data Sheet Errata

The PIC16C63A/65B/73B/74B parts you have received conform functionally to the Device Data Sheet (DS30605**C**), except for the anomalies described below.

1. Module: RESET

The minimum specification for the $\overline{\text{MCLR}}$ must be met in order to reset the PIC16CXXX. If a $\overline{\text{MCLR}}$ pulse occurs that is less that the minimum specification (parameter #30), improper device operation can occur.

If the minimum specification cannot be met, then an external circuit must be used to ensure that any pulse width less than the specification will be filtered before it reaches the $\overline{\text{MCLR}}$ pin.

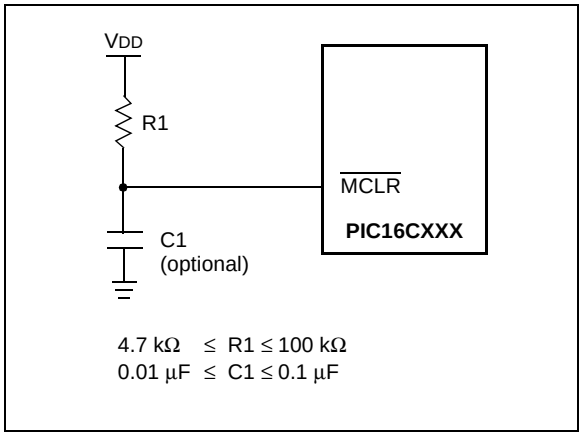
Work around

A possible circuit is shown in Figure 1. This circuit works by delaying the $\overline{\text{MCLR}}$ release following a power-up. If no delay is required, the capacitor may be omitted.

An alternative would be to use a supervisory circuit to control $\overline{\text{MCLR}}$.

Design validation should be performed to verify that the application works as expected.

FIGURE 1: $\overline{\text{MCLR}}$ EXTERNAL CIRCUIT



2. Module: OSCILLATOR

The Oscillator Start-up Timer (TOST) delay may not occur when the device wakes up from SLEEP.

Figure 2 shows the start-up of the crystal after the event that causes the device to wake-up from SLEEP mode (as specified in device data sheet). The start-up time (TOST) may not occur.

The events that wake-up the device from SLEEP are:

- An interrupt
- A WDT overflow (wake-up)
- A Brown-out Reset
- A $\overline{\text{MCLR}}$ Reset

In applications where time-based measurements are started immediately after wake-up from SLEEP, the suggested work around should be implemented.

Work around

After the SLEEP instruction, do a software delay of 256 TCY (same as 1024 TOSC). At the RESET and Interrupt vector addresses, test to see if the device woke from SLEEP (the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits), and if the device did wake from SLEEP, ensure that the total cycle delay is 256 TCY.

3. Module: TMR1

When operating in External Clock mode (TMR1CS is set), reading either of the Timer 1 registers (TMR1H or TMR1L) may cause the timer not to increment as expected. This occurs for both synchronous and asynchronous inputs.

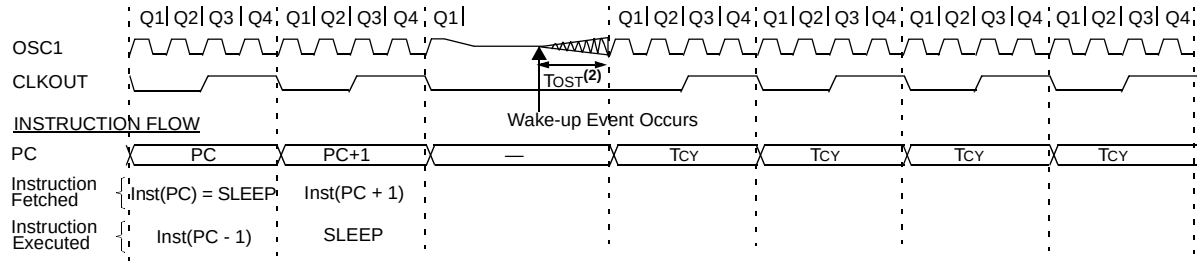
The scenarios which display this are:

- When a read operation of the TMR1H register occurs, the TMR1L register may not increment.
- When a read operation of the TMR1L register occurs, the TMR1H register may not increment. This improper operation is only an issue when the TMR1L register increments from FFh to 00h (FFh → 00h), during the read of the TMR1L register.

Work around

Do not read either the TMR1H or the TMR1L registers when operating in External Clock mode (TMR1CS is set). If the application needs to read the 16-bit counter, evaluate if this function can be moved to the TMR0, or one of the other timer resources on the device.

FIGURE 2: WAKE-UP FROM SLEEP



Note 1: For TOST delay to be enabled, the XT, HS or LP Oscillator mode must be selected.
2: TOST = 1024 TOSC. This delay may not occur, and every valid clock edge will generate internal device clocks.
3: CLKOUT is not available in these osc modes, but shown here for timing reference.

Clarifications/Corrections to the Data Sheet:

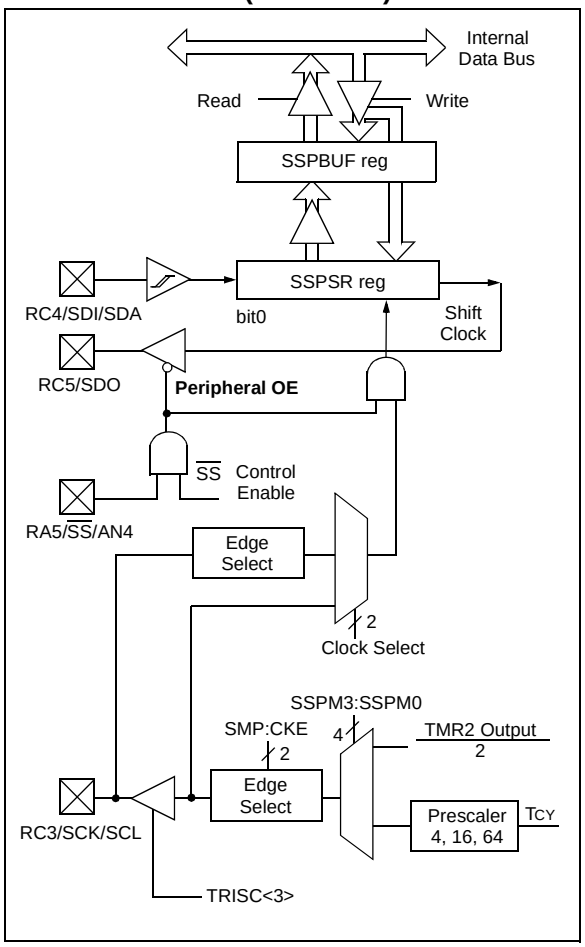
In the Device Data Sheet (DS30605**C**), the following clarifications and corrections should be noted:

1. Module: SSP (SPI™ Mode)

In Section 10.2 (“SPI Mode”), Figure 10-1 and the note box immediately beneath it have been amended to better demonstrate the Peripheral OE line of the SSP module and describe its relationship to the TRISC<5> bit of PORTC.

Changes are indicated in **bold**.

FIGURE 10-1: SSP BLOCK DIAGRAM (SPI MODE)



Note 1: When the SPI module is in Slave mode with $\overline{SS}$ pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the $\overline{SS}$ pin is set to VDD.

2: If the SPI is used in Slave mode with CKE = '1', then $\overline{SS}$ pin control must be enabled.

3: When the SPI is in Slave mode with $\overline{SS}$ pin control enabled (SSPCON<3:0> = 0100), the state of the SS pin can affect the state read back from the TRISC<5> bit. The Peripheral OE signal from the SSP module into PORTC, controls the state that is read back from the TRISC<5> bit (see Section 5.3 for information on PORTC). If Read-Modify-Write instructions, such as BSF, are performed on the TRISC register while the SS pin is high, this will cause the TRISC<5> bit to be set, thus disabling the SDO output.

APPENDIX A: REVISION HISTORY

Rev B Document (10/2001)

Issues 1, 2 and 3 (RESET, Oscillator and Timer1 modules) were added, pages 1 and 2.

Under Clarifications/Corrections to the Data Sheet, all issues referenced pertain to Revision ‘C’ of the Data Sheet instead of Revision ‘A’.

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