PIC16C73A → PIC16C73B Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences and the electrical specification differences that are present when migrating from one device to the next.

Note:	This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

Note:	The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

Table 1 shows the considerations that must be taken into account when migrating from the PIC16C73A to the PIC16C73B.

TABLE 1: PIC16C73A → PIC16C73B DIFFERENCES

Functional Differences due to Errata or Module Update					
No.	**Module**	**Difference**	**H/W**	**S/W**	**Prog.**
1	CCP	CCP Special Event Trigger clears Timer1.	—	✓	—
2		Compare mode drives pin correctly.	—	✓	—
3	Timers	Reading or writing TMR1L or TMR1H may affect TMR1L or TMR1H unexpectedly.	—	✓	—
4		WDT/TMR0 prescaler assignment changes do not affect TMR0 count.	—	✓	—
5	SSP	TMR2 SPI™ clock synchronized to start of SPI Transmission.	—	✓	—
6		Can now transmit multiple words in SPI mode.	—	✓	—
7		Supports all four SPI modes. (Now uses SSP vs BSSP module.) See SSP module in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).	—	✓	—
8		I^2C™ no longer generates ACK pulses when module is enabled.	—	✓	—
9	USART	Async receive errors due to BRGH setting corrected.	—	✓	—
10	Oscillator	TOST delay may be skipped when waking from SLEEP.	—	✓	—
11	RESET	Short $\overline{MCLR}$ pulses may cause improper operation.	✓	—	—
12		Operating voltage and frequency ranges have been redefined.	✓	—	—
13	A/D	Digital inputs may be converted if any pin is configured as an analog input.	—	✓	—

H/W - Issues may exist with regard to the application circuits.
S/W - Issues may exist with regard to the user program.
Prog. - Issues may exist when writing the program to the controller.

TABLE 2: ELECTRICAL SPECIFICATION DIFFERENCES

Param No.	Symbol	Characteristic		PIC16C73A			PIC16C73B			Unit
				Min	Typ†	Max	Min	Typ†	Max	
Core										
D001	VDD	Supply Voltage XT, LP and RC mode		4.0	—	6.0	4.0	—	**5.5**	V
D001A		HS mode		4.5	—	6.0	**4.0**	—	**5.5**	V
		BOR enabled **(Note 1)**		—	—	—	**VBOR**	—	**5.5**	V
D005	VBOR	Brown-out Reset Voltage		3.7	4.0	4.3	**3.65**	—	**4.35**	V
D150	VOD	Open Drain High Voltage on RA4		—	—	14.0	—	—	**8.5**	V
A/D Converter										
A20	VREF	Reference Voltage		3.0	—	VDD + 0.3	**2.5**	—	VDD + 0.3	V
131	TCNV	Conversion time **(Note 2)** (not including S/H time)		—	9.5 **(Note 3)**	—	**11 (Note 4)**	—	**11 (Note 4)**	TAD
SSP in SPI mode										
71	TscH	SCK input high time (Slave mode)	Continuous	TCY+20	—	—	**1.25TCY + 30**	—	—	ns
71A			Single Byte				**40**	—	—	ns
72	TscL	SCK input low time (Slave mode)	Continuous	TCY+20	—	—	**1.25TCY + 30**	—	—	ns
72A			Single Byte				**40**	—	—	ns
73	TdiV2scH TdiV2scL	Setup time of SDI data input to SCK edge		—	—	—	**100**	—	—	ns
73A **(Note 5)**	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		100	—	—	**1.5TCY + 40**	—	—	ns
74	TscH2diL TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	**100**	—	—	ns
75	TdoR	SDO data output rise time	PIC16CXX	—	10	25	—	10	25	ns
			PIC16LCXX				—	**20**	**45**	ns
78	TscR	SCK output rise time (Master mode)	PIC16CXX	—	10	25	—	10	25	ns
			PIC16LCXX				—	**20**	**45**	ns
80	TscH2doV TscL2doV	SDO data output valid after SCK edge	PIC16CXX	—	—	50	—	—	50	ns
			PIC16LCXX				—	—	**100**	ns
83	TscH2ssH TscL2ssH	$\overline{SS}$ ↑ after SCK edge		—	—	—	**1.5TCY + 40**	—	—	ns

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When BOR is enabled, the device will operate until VDD drops below VBOR.
2: ADRES register may be read on the following TCY cycle.
3: This is the time that the actual conversion requires.
4: This is the time from when the GO/$\overline{DONE}$ bit is set to when the conversion result appears in ADRES.
5: Specification 73A is only required if specifications 71A and 72A are used.

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AMERICAS

Corporate Office
2355 West Chandler Blvd.
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Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Austin - Analog
13740 North Highway 183
Building J, Suite 4
Austin, TX 78750
Tel: 512-257-3370 Fax: 512-257-8526

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Boston - Analog
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Concord, MA 01742
Tel: 978-371-6400 Fax: 978-371-0050

Chicago
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Tel: 630-285-0071 Fax: 630-285-0075

Dallas
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Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton
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Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Rm. 531, North Building
Fujian Foreign Trade Center Hotel
73 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7557563 Fax: 86-591-7557572

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Denmark ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Germany - Analog
Lochhamer Strasse 13
D-82152 Martinsried, Germany
Tel: 49-89-895650-0 Fax: 49-89-895650-22

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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