PIC16F87XA → PIC16F88X Migration

DEVICE MIGRATIONS

This document provides an overview of considerations for migrating from the PIC16F87XA product family to the PIC16F88X devices. When undertaking this migration, we recommended downloading data sheets and errata documents on these devices from our web site, located at http://www.microchip.com.

Note 1: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

2: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required.

Table 1 shows the considerations that must be taken into account when migrating from the PIC16F87XA to the PIC16F88X.

TABLE 1: PIC16F87XA → PIC16F88X MIGRATION DIFFERENCES

Functional Differences				
No.	**Difference**	**H/W**	**S/W**	**Prog.**
1	Ports A, B, and E		✔	
2	Weak pull-ups are individually configurable		✔	
3	WDT (Time-out period may be extended)		✔	
4	Timer1 with gate control		✔	
5	2 independent analog comparators	✔	✔	
6	ECCP and CCP		✔	
7	Additional A/D channels		✔	
8	Enhanced USART with auto-baud		✔	
9	Configuration Word		✔	
10	BOR voltage is selectable		✔	
11	Program Flash memory write		✔	
12	Parallel slave port	✔	✔	
Legend:	H/W – Issues may exist with regard to the application circuit. S/W – Issues may exist with regard to the user program. Programming – Issues may exist with regard to programming the device.			

CODE CONVERSION

The vast majority of the code that was developed for the PIC16F87XA family is portable to its corresponding PIC16F88X counterpart. However, in some cases, some changes may be required depending on which feature set is being used. To migrate source code to the PIC16F88X, the following steps must be performed:

1. Replace the PIC16F87XA include file with the corresponding PIC16F88X include file.
2. Configure the ANSEL and ANSELH registers to assure proper operation of PORTA, PORTB and PORTE. The ANSEL and ANSELH registers default state disables the digital input buffer forcing these port pins to always read as '0'.
3. Any source code that made use of the Parallel Slave Port (PSP) peripheral will need to be rewritten. The PSP peripheral does not exist in the PIC16F88X product family.
4. Make the necessary changes to the new or enhanced peripherals that are being used, as listed below.
5. Verify the Configuration bits are set properly.

PORTA

The ANSEL register is used to configure the Input mode of pins AN<7:0>, respectively. If an analog function is required on AN<4:0> the corresponding bit of the ANSEL register should be set. Once the ANSEL bit is set the digital input driver will be disabled and the corresponding PORTA bit, if read, will read as '0'. By default ANSEL is 0FFh. For a pin on PORTA to operate as a digital input, the corresponding ANSEL bit must be cleared. ANSEL has no effect on the output functionality of PORTA.

RA0 has the ULPWU (ultra low-power wake-up) multiplexed on the pin. The ULPWU is enabled by setting the ULPWUE bit of the PCON register. By default the ULPWU is off.

RA6 and RA7 are new pins for PORTA. In XT, HS or LP Clock modes these port pins will act as unimplemented pins and will read as '0'. In RCIO Clocking mode RA6 will function as an IO.

PORTB

The ANSELH register is used to configure the Input mode of pins AN<13:8>, respectively. If an analog function is required on AN<13:7> the corresponding bit of the ANSEL register should be set. Once the ANSELH bit is set, the digital input driver will be disabled and the corresponding PORTB bit, if read, will read as '0'. By default ANSELH is 0FFh. For a pin on PORTB to operate as a digital input, the corresponding ANSELH bit must be cleared. ANSELH has no effect on the output functionality of PORTB.

PORTE

The ANSEL register is used to configure the Input mode of pins AN<7:0>, respectively. If an analog function is required on AN<7:5> the corresponding bit of the ANSEL register should be set. Once the ANSEL bit is set, the digital input driver will be disabled and the corresponding PORTE bit, if read, will read as '0'. By default ANSEL is 0FFh. For a pin on PORTE to operate as a digital input, the corresponding ANSEL bit must be cleared. ANSEL has no effect on the output functionality of PORTE.

RE3 is a new input only pin to PORTE. When configured for external $\overline{MCLR}$, RE3 acts as an unimplemented pin and always reads as '0'.

WEAK PULL-UPS ON PORTB

The weak pull-ups on PORTB now have individual control via the WPUB register. Clearing the RBPU bit of the OPTION register, the weak pull-up feature is enabled. By default all individual weak pull-ups will be enabled. No software changes should be needed for this feature to operate as intended.

INTERRUPT-ON-CHANGE PORTB

The IOC on PORTB now has individual control via the IOCB register. Setting the RBIE bit of the INTCON register enables the IOC feature. By default, all individual interrupt-on-change are disabled. For software compatibility the following should be written to the IOCB register:

EXAMPLE 1: COMPATIBILITY FOR INTERRUPT-ON-CHANGE PORTB

```
IOCB        b'11111111'
```

EXTENDED WATCHDOG TIMER (WDT)

The WDTCON register is a new register to allow more flexibility in the watchdog time-out period. The WDTCON register in conjunction with the shared prescaler of Timer0, allows the time-out period to vary from 1ms to 268 seconds. The default setting of the WDTCON register sets the time-out period to be 17 ms with no prescaler. No software changes are required to have the watchdog time-out period to stay the same.

TIMER1 WITH GATE ENABLE

Two bits have been added to the T1CON register which were previously unimplemented. Bit 6 (TMR1GE) selects if Timer1 is gated by the T1G pin and bit 7 (T1GINV) changes the T1G pin from being active-high to active-low. By default, TMR1GE is off. Source code must have bit 6 of T1CON cleared in order for Timer1 to not be effected by the TMR1GE function.

EXAMPLE 2: TIMER1 WITH GATE ENABLE

```
T1CON      b'x0xxxxxx'
```

COMPARATOR MODULES

The comparator module has changed from the PIC16F87XA to the PIC16F88X. The Comparator modes have been removed in favor of having two independent comparators. Each comparator has a separate control register and the old CMCON register of PIC16F87XA no longer exists. For each Comparator mode, the new settings should be as follows:

Note 1: CMCON of the PIC16F87XA is in bank 1. CM1CON0, CM2CON0 and CM2CON1 of the PIC16F88X are in bank 2.

2: The SRCON register should be left in its default state of 00h.

3: CVRCON register has been renamed VRCON and it was moved from address 9Dh to 97h in the memory map. The functionality of CVRCON has not changed.

EXAMPLE 3: MODE 000: COMPARATOR RESET

```
CM1CON0    b'00000000' (default)
CM2CON0    b'00000000' (default)
CM2CON1    02h (default)
ANSEL      b'xxxx1111'
```

EXAMPLE 4: MODE 001: ONE INDEPENDENT COMPARATOR WITH OUTPUT

```
CM1CON0    b'10100100'
CM2CON0    b'00000000' (default)
CM2CON1    02h (default)
ANSEL      b'xxxx1001'
```

EXAMPLE 5: MODE 010: TWO INDEPENDENT COMPARATORS

```
CM1CON0    b'100x0000'
CM2CON0    b'100x0001'
CM2CON1    02h (default)
ANSEL      b'xxxx1111'
```

EXAMPLE 6: MODE 011: TWO INDEPENDENT COMPARATORS WITH OUTPUTS

```
CM1CON0    b'101x0000'
CM2CON0    b'101x0001'
CM2CON1    02h (default)
ANSEL      b'xxxx1111'
```

EXAMPLE 7: MODE 100: TWO COMMON REFERENCE COMPARATORS

```
CM1CON0    b'100x0000'
CM2CON0    b'100x0001'
CM2CON1    02h (default)
ANSEL      b'xxxx1011'
```

Comparator 2 will not function properly if this is the mode previously used. The positive input of comparator 2 cannot be mapped to the positive input of comparator 1 via software. The following settings have the positive input of comparator 2 mapped to RA2.

EXAMPLE 8: MODE 101: TWO COMMON REFERENCE COMPARATORS WITH OUTPUTS

```
CM1CON0    b'101x0000'
CM2CON0    b'101x0001'
CM2CON1    02h (default)
ANSEL      b'xxxx1011'
```

Comparator 2 will not function properly if this is the mode previously used. The positive input of comparator 2 cannot be mapped to the positive input of comparator 1 via software. The following settings have the positive input of comparator 2 mapped to RA2.

EXAMPLE 9: MODE 110: FOUR INPUTS MULTIPLEXED TO TWO COMPARATORS.

```
CM1CON0     b'100x0100'
CM2CON0     b'100x0101'
CM2CON1     32h
ANSEL       b'xxxx1111'
```

Comparator 1 and comparator 2 may not function properly if this is the mode previously used. The negative input of comparator 1 can not be mapped to RA3 and the negative input of comparator 2 can not be mapped to RA2 via software. The following settings have the negative input of comparator 1 mapped to RA0 and the negative input of comparator 2 mapped to RA1.

EXAMPLE 10: MODE 111: COMPARATORS OFF

```
CM1CON0     b'00000000' (default)
CM2CON0     b'00000000' (default)
CM2CON1     02h (default)
ANSEL       b'xxxx0000'
```

ANALOG-TO-DIGITAL CONVERTER

There are three major changes with the A/D module that affect the ADCON0 and ADCON1 registers.

1. One conversion clock select bit was removed from ADCON1, leaving 4 clock selections to time an A/D conversion.
2. One additional channel select bit was added to ADCON0 to allow selection of channels AN9-AN13.
3. The port Configuration bits of ADCON1 register have been removed. Determination of analog or digital for and individual pin is now provided by the ANSELH:ANSEL register pair. If an analog function is required on AN<13:0> the corresponding bit of the ANSELH:ANSEL register pair should be set. Once the bit is set, the digital input driver of the corresponding port pin will be disabled. By default ANSELH and ANSEL are 0FFh.

To implement these changes both ADCON0 and ADCON1 have been redefined. These registers along with the ANSELH and ANSEL registers will have to be reconfigured to get a proper conversion.

REGISTER 1: ADCON0

ADCS1	ADCS0	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable’	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **ADCS<1:0>:** A/D Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max.)

bit 5-2 **CHS<3:0>:** Analog Channel Select bits
0000 = AN0
0001 = AN1
.
.
.
1101 = AN13
1110 = CVREF
1111 = Fixed Ref (0.6 volt fixed reference)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bits
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle. This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

REGISTER 2: ADCON1

ADFM	—	VCFG1	VCFG1	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable’	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Conversion Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **VCFG1:** Voltage Reference bit
1 = VREF- pin
0 = VSS

bit 4 **VCFG1:** Voltage Reference bit
1 = VREF+ pin
0 = VDD

bit 3-0 **Unimplemented:** Read as ‘0’

ECCP AND CCP MODULES

The only change to the CCP modules is in the PWM mode of CCP1. No changes have been made to the Capture or Compare modes of the CCP or ECCP. Bits 7 and 6 of the CCP1CON register, which were previously unimplemented, have been added to control the P1B, P1C and P1D outputs. These outputs are typically used for driving a Half Bridge or Full Bridge and are only active in CCP1's PWM mode. To disable the P1B, P1C and P1D outputs, bits 7 and 6 of CCP1CON should be cleared.

EXAMPLE 11: CLEARING CCP1CON BITS 7 AND 6

```
CCP1CON     b'00xxxxxx'
```

EUSART WITH AUTO-BAUD

The baud rate of EUSART is controlled by the 16-bit SBRGH:SPBRG register pair. Previously the AUSART baud rate was controlled by the 8-bit SPBRG register. To have the EUSART operate at the same baud rate of the AUSART, both the SPBRGH and the BRG16-bit of the BAUDCTL register must be cleared.

The EUSART also incorporates Auto-Baud Detection. Auto-baud is controlled exclusively by the BAUDCTL register and the SENDB bit of TXSTA. To disable this feature both the SENDB bit of the TXSTA register and the BAUDCTL register must remain cleared.

EXAMPLE 12:

```
TXSTA       b'xxxx0xxx'
SPBRGH      b'00000000'
BAUDCTL     b'00000000'
```

PROGRAM FLASH MEMORY WRITE

	PIC16F87XA	PIC16F882/ 883/884	PIC16F886/887
Erase Size	4 words	16 words	16 words
Write Block Size	4 words	4 words	8 words

Writing to program memory for the PIC16F88X parts is performed in multiple block write to a row. A block consists of either four or eight words of sequential addresses and a row is defined as 16 words with the first address as EEADR<3:0>=0000. To write a row, you must write blocks sequentially starting at the first address of the row. The first block written to a row erases the entire row. Consecutive block writes to the same row will not cause an additional row erase. All other aspects of the Program Flash Memory Write remain the same.

CONFIGURATION WORDS

The Configuration Word of the PIC16F87XA product family has been expanded to two Configuration Words. Below are the definitions of the two Configuration Words for the PIC16F88X product family, verify they are set properly.

BROWN OUT DETECT

The Brown-out Detect circuit now has 2 separate voltages in which it can operate at, either 2.1 volts or 4.0 volts. Determination of the Brown-out trip point is determined by the setting of the BOR4 bit of Configuration Word 2. To enable the Brown-out Detect, there are now 3 different modes:

EXAMPLE 13: BROWN-OUT RESET - CONFIGURATION WORD 1

bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits(1)

11 = BOR enabled

10 = BOR enabled during operation and disabled in Sleep

01 = BOR controlled by SBOREN bit of the PCON register

00 = BOR disabled

Note 1: It is recommended for compatibility to have the BOREN<1:0> set to '11'.

REGISTER 3: CONFIG: CONFIGURATION WORD REGISTER

—	—	DEBUG	LVP	FCMEN	IESO	BOREN1	BOREN0
bit 15							bit 8

$\overline{CPD}$	$\overline{CP}$	MCLRE	$\overline{PWRTE}$	WDTE	FOSC2	FOSC1	FOSC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable'	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented**: Read as '1'

bit 13 **DEBUG:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, RB6/CSPCLK and RB7/ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, RB6/CSPCLK and RB7/ICSPDAT are dedicated to the debugger

bit 12 **LVP:** Low Voltage Programming Enable bit
1 = RB3/PGM pin has PGM function, low voltage programming enabled
0 = RB3 pin is digital I/O, HV on $\overline{MCLR}$ must be used for programming

bit 11 **FCMEN:** Fail-Safe Clock Monitor Enabled bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 10 **IESO:** Internal External Switchover bit
1 = Internal External Switchover mode is enabled
0 = Internal External Switchover mode is disabled

bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits**(1)**
11 = BOR enabled, SBOREN bit disabled
10 = BOR enabled during operation and disabled in Sleep, SBOREN bit disabled
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR and SBOREN bits disabled

bit 7 **$\overline{CPD}$:** Data Code Protection bit**(2)**
1 = Data memory code protection is disabled
0 = Data memory code protection is enabled

bit 6 **$\overline{CP}$:** Code Protection bit**(3)**
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 5 **MCLRE:** $\overline{MCLR}$ pin function select bit**(4)**
1 = $\overline{MCLR}$ pin function is $\overline{MCLR}$
0 = $\overline{MCLR}$ pin function is digital input, $\overline{MCLR}$ internally tied to V_{DD}

bit 4 **$\overline{PWRTE}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled and can be enabled by SWDTEN bit of the WDTCON register

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = EXTRC oscillator: External RC on RA5/OSC1/CLKIN, CLKOUT function on RA4/OSC2/CLKOUT pin
110 = EXTRCIO oscillator: External RC on RA5/OSC1/CLKIN, I/O function on RA4/OSC2/CLKOUT pin
101 = INTOSC oscillator: CLKOUT function on RA4/OSC2/CLKOUT pin, I/O function on RA5/OSC1/CLKIN
100 = INTOSCIO oscillator: I/O function on RA4/OSC2/CLKOUT pin, I/O function on RA5/OSC1/CLKIN
011 = EC: I/O function on RA4/OSC2/CLKOUT pin, CLKIN on RA5/OSC1/CLKIN
010 = HS oscillator: High-speed crystal/resonator on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN
001 = XT oscillator: Crystal/resonator on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN
000 = LP oscillator: Low-power crystal on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire data EEPROM will be erased when the code protection is turned off.
3: The entire program memory will be erased when the code protection is turned off.
4: When $\overline{MCLR}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

REGISTER 4: CONFIG2: CONFIGURATION WORD REGISTER 2

—	—	—	—	—	WRT1	WRT0	BOR4V
bit 15							bit 8

—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable’	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented**: Read as ‘1’

bit 10-9 **WRT<1:0>:** Flash Program Memory Self Write Enable bits

PIC16F883/PIC16F884

00 = 0000h to 07FFh write-protected, 0800h to 0FFFh may be modified by EECON control

01 = 0000h to 03FFh write-protected, 0400h to 0FFFh may be modified by EECON control

10 = 0000h to 00FFh write-protected, 0100h to 0FFFh may be modified by EECON control

11 = Write protection off

PIC16F886/PIC16F887

00 = 0000h to 0FFFh write-protected, 1000h to 1FFFh may be modified by EECON control

01 = 0000h to 07FFh write-protected, 0800h to 1FFFh may be modified by EECON control

10 = 0000h to 00FFh write-protected, 0100h to 1FFFh may be modified by EECON control

11 = Write protection off

PIC16F882

00 = 0000h to 07FFh write-protected, entire program memory is write protected

01 = 0000h to 03FFh write-protected, 0100h to 07FFh may be modified by EECON control

10 = 0000h to 00FFh write-protected, 0100h to 07FFh may be modified by EECON control

11 = Write protection off

bit 8 **BOR4V**: Brown-out Reset Selection bit

0 = Brown-out Reset set to 2.1V

1 = Brown-out Reset set to 4.0V

bit 7-0 **Unimplemented**: Read as ‘1’

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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