PIC18FXX8

PIC18FXX8 Rev. B4 Silicon Errata Sheet

The PIC18FXX8 Rev. B4 parts you have received conform functionally to the Device Data Sheet (DS41159**D**), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC18FXX8 silicon.

The following silicon errata apply only to PIC18FXX8 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F248	00 1000 000	00100
PIC18F258	00 1000 010	00100
PIC18F448	00 1000 001	00100
PIC18F458	00 1000 011	00100

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: ECCP

When the ECCP module is operating in Half-Bridge mode, use of a dead-band delay other than zero will have the effect of introducing an unintended pulse on the P1A and P1B signals.

Work around

Disable the dead-band delay by ensuring that the ECCP1DEL register is set to 00h.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: I/O (Parallel Slave Port)

The Input Buffer Status bit of the TRISE register (TRISE<7>) may be inadvertently cleared, even when the PORTE input buffer has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = 1111) and
- Any instruction that contains 83h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh. In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the Access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select Banks 1 through 5 and the upper half of Bank 0.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain 83h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

3. Module: Core (Program Memory Space)

Performing table read operations above the user program memory space (addresses over 1FFFFFh) may yield erroneous results at the extreme low end of the device's rated temperature range (-40°C).

This applies specifically to addresses above 1FFFFFh, including the user ID locations (200000h-200007h), the configuration bytes (300000h-30000Dh) and the device ID locations (3FFFFEh and 3FFFFFh). User program memory is unaffected.

Work around

Two possible work arounds are presented. Other solutions may exist.

1. Do not perform table read operations on areas above the user memory space at -40°C.
2. Insert NOP instructions (specifically, literal FFFFh) around any table read instructions. The suggested optimal number is 4 instructions before and 8 instructions after each table read. This may vary, depending upon the particular application and should be optimized by the user.

Date Codes that pertain to this issue::

All engineering and production devices.

4. Module: Core (Program Memory Space)

Note:	This issue applies **only** to PIC18F258 and PIC18F458 devices with 32 Kbytes of Flash program memory. PIC18F248 and PIC18F448 devices are **not** affected.

Under certain conditions, the execution of a table read instruction may yield erroneous results. This has been observed when a table read instruction and its read destination, as indicated by the Table Pointer registers, are on opposite sides of the 4000h program memory address boundary.

This behavior has not been observed when the instruction and its target both occur strictly within the same half of the program memory space.

Work around

Insert a data word of value FFFFh immediately following any table read instruction. This behaves as a NOP instruction when executed. Using the actual NOP instruction instead of a literal FFFFh may not have the same results.

This is a recommended solution. Others may exist.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Core (Program Memory Space)

Note:	This issue applies **only** to PIC18F258 and PIC18F458 devices with 32 Kbytes of Flash program memory. PIC18F248 and PIC18F448 devices are **not** affected.

Under certain conditions, the execution of some control operations may yield unexpected results. This has been observed when the following instructions vector code execution across the 4000h program memory address boundary:

- CALL
- GOTO
- RETURN
- RETLW
- RETFIE

There are no known issues related to any of these instructions when execution occurs strictly above or below the 4000h address boundary.

Work around

Two possible solutions are presented. Others may exist. It is recommended to implement either or both as needed.

1. Insert a data word of value FFFFh as the first instruction in the destination of a CALL or GOTO.
2. Insert a data word of value FFFFh immediately following any RETURN, RETLW or RETFIE instruction.

In either case, the literal data behaves as a NOP instruction when executed. Using the actual NOP instruction instead of a literal FFFFh may not have the same results.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Data EEPROM

When reading the data EEPROM, the contents of the EEDATA register may be corrupted if the RD bit (EECON1<0>) is set immediately following a write to the address byte (EEADR). The actual contents of the data EEPROM remain unaffected.

Work around

Do not set EEADR immediately before the execution of a read. Write to EEADR at least one instruction cycle before setting the RD bit. The instruction between the write to EEADR and the read can be any valid instruction, including a NOP.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: A/D (External Voltage Reference) and Comparator Voltage Reference

When the external voltage reference, VREF-, is selected for use with either the A/D or comparator voltage reference, AVSS is connected to VREF- in the comparator module. If VREF- is a voltage other than AVSS (which must be tied externally to VSS), excessive current will flow into the VREF- pin.

Work around

If external VREF- is used with a voltage other than 0V, enable the comparator voltage reference by setting the CVREN bit in the CVRCON register. This disconnects VREF- and AVSS within the comparator module.

8. Module: CAN

CAN Disable mode change request is not confirmed. A CAN Disable mode request by writing '001' to the REQOP bits (CANCON<5:7>) immediately changes the OPMODE bits (CANSTAT<5:7>), implying that Disable mode is accepted. This occurs even though the CAN module itself may not have switched its state.

Work around

Switch to Configuration mode instead. Wake-up from CAN bus activity will continue to work even in Configuration mode.

9. Module: MSSP (All I²C™ and SPI™ Modes)

The Buffer Full (BF) flag bit of the SSPSTAT register (SSPSTAT<0>) may be inadvertently cleared even when the SSPBUF register has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = 1111) and
- Any instruction that contains C9h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh.

In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select all GPR Banks.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain C9h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: MSSP (SPI, Slave Mode)

In its current implementation, the $\overline{SS}$ (Slave Select) control signal generated by an external master processor may not be successfully recognized by the PIC® microcontroller operating in Slave Select mode (SSPM3:SSPM0 = 0100). In particular, it has been observed that faster transitions (those with shorter fall times) are more likely to be missed than than slower transitions.

Work around

Insert a series resistor between the source of the $\overline{SS}$ signal and the corresponding $\overline{SS}$ input line of the microcontroller. The value of the resistor is dependent on both the application system's characteristics and process variations between microcontrollers. Experimentation and thorough testing are encouraged.

This is a recommended solution. Others may exist.

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: CAN

An incoming CAN message may not be saved properly to a CAN receive buffer if one of the following conditions is met:

1. Bank 15 is selected and the firmware attempts to read RXB0 or RXB1 registers while a CAN message reception is in progress.
2. Bank 15 is selected and an instruction is executed whose lower 8 bits match with one of the CAN receive buffer addresses (RXBn addresses in the range of 0xF61 to 0xF6E and 0xF51 to 0xF5D) while a CAN message reception is in progress. Some of the instruction examples are:
   - 0xFF68 (NOP)
   - 0xEE68 (first half of GOTO 0xD0)
   - 0x0E6A (MOVLW 0x6A)
   - 0x6055 (MOVF 0xF66, W)

   Other instruction combinations exist.
3. The firmware attempts to access GPRs (General Purpose Register addresses) between addresses 0x51 and 0x5D in the Access Bank while a CAN message reception is in progress. Some of the instruction examples are:
   - MOVWF 0x57, A
   - ADDWF 0x57, A
   - MOVF 0x57, W, A

Work around

1. Once in normal CAN module mode, never select Bank 15. Always use Access Bank RAM to access the CAN buffers. The RXB0 buffer is already available in the Access Bank. All other transmit and receive buffers are available in Access Bank RAM, via the RXB0 registers, using the WIN bits available in the CANCON register.
2. Always make sure that the RXFUL bit is set before attempting to access any of the receive buffer registers.
3. Do not access/use any of the registers in the Access Bank address range of 0x051 to 0x05D. If using assembly language, do not allocate any of your application variables in this address range. If using C compiler, make sure that the compiler does not allocate any variable in the specified address range.

12. Module: Reset

It has been observed that in certain Reset conditions, including power-up, the first GOTO instruction at address 0x0000 may not be executed. This occurrence is rare and affects very few applications.

To determine if your system is affected, test a statistically significant number of applications across the operating temperature, voltage and frequency ranges of the application. Affected systems will repeatably fail normal testing. Systems not affected will continue to not be affected over time.

Work around

Insert a NOP instruction at address 0x0000.

Date Codes that pertain to this issue:

All engineering and production devices.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41159**D**), the following clarifications and corrections should be noted.

None.

REVISION HISTORY

Rev A Document (7/2002)

First revision of this document, silicon issues 1 (ECCP), 2 (I/O – Parallel Slave Port) and 3 (Core – Program Memory Space).

Rev B Document (11/2002)

Added silicon issues 4, 5, 6 and 7 (Core – Program Memory Space and Data EEPROM).

Rev C Document (03/2003)

Added silicon issue 7 (A/D (External Voltage Reference) and Comparator Voltage Reference) and data sheet clarification issue 1 (A/D – VREF+ and VREF- References).

Rev D Document (03/2004)

Added silicon issue 8 (CAN), 9 (MSSP – All I^2C and SPI Modes) and 10 (MSSP – SPI, Slave Mode). Added data sheet clarification issues 2 (External Clock Timing Requirements – Table 27-6), 3 (A/D Converter Characteristics – Table 27-23) and 4 (Comparator Voltage Reference Module).

Rev E Document (09/2004)

Added silicon issue 11 (CAN).

Rev F Document (11/2004)

Updated silicon issue 11 (CAN) and removed all Data Sheet Clarification issues.

Rev G Document (05/2005)

Added silicon issue 12 (Reset).

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