Replacing SRAM with FRAM

Parallel FRAM Design Considerations

Ramtron offers three FRAM devices that are pin compatible with industry standard bytewide (x8) SRAMs. The FM1608 is an 8Kx8 and the FM1808 and FM18L08 are 32Kx8 devices, all of which may be used as non-volatile SRAM replacements. This application note highlights some design considerations which we recommend you review prior to finalizing your design.

Confirm Operation of Chip Enable

SRAM and FRAM alike begin each read/write cycle with a new address being driven prior to the chip enable transition low. The falling edge of chip enable latches the address and a memory access starts. For subsequent memory accesses, SRAMs allow /CE to remain low while the address bus changes. FRAM devices do not allow this signalling. Every FRAM access requires a falling edge of /CE, therefore users cannot ground this pin as you might with SRAM.

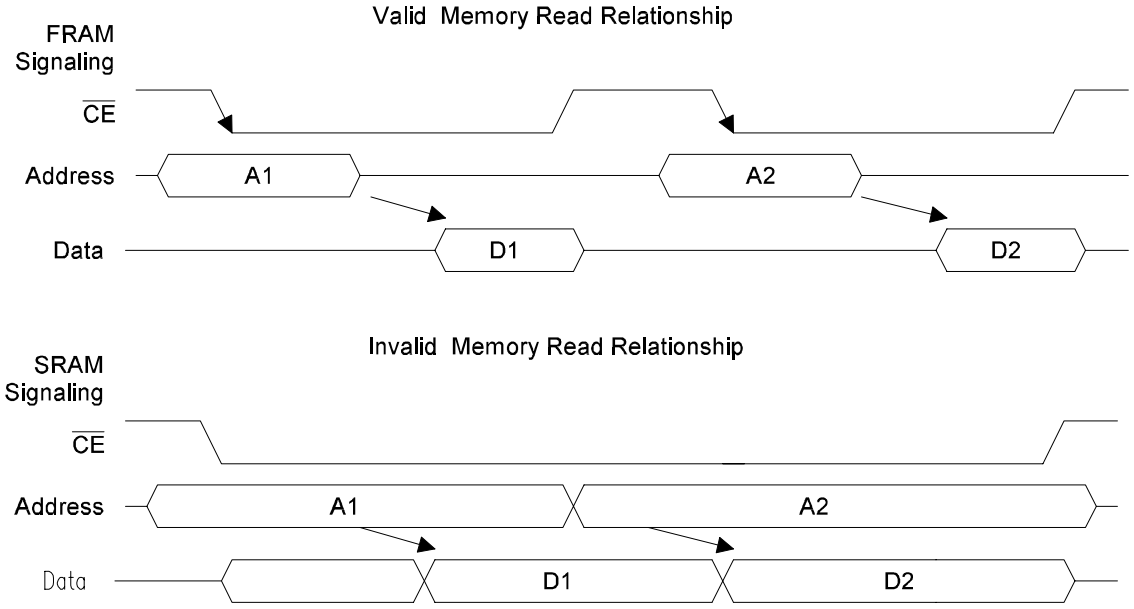
Users who are modifying existing designs to use FRAM should examine the memory controller for timing compatibility of address and control pins. Each memory access must be qualified with a low transition of /CE. In many cases, this is the only change required. An example of the signal relationships is shown below.

Also shown is a common SRAM signal relationship that will not work for the FRAM devices.

The reason for /CE to strobe for each address is two-fold: it latches the new address and creates the necessary precharge period while /CE is high.

Confirm Power Supply Level

A second design consideration relates to the level of V_{DD} during operation. Battery-backed SRAMs are designed to monitor V_{DD} in order to switch to battery backup. They typically block user access below a certain V_{DD} level in order to minimize battery drain from an otherwise active SRAM. The user can be abruptly cut off from access to the memory in a power down situation without warning. FRAM memories do not need this system overhead. The memory will not block access at any V_{DD} level. The user, however, should prevent the processor from accessing memory when V_{DD} is out-of-tolerance. Check the min/max V_{DD} specifications on FRAM datasheet. The common design practice of holding a processor in reset when V_{DD} drops is sufficient. No special provisions must be taken for FRAM design.



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