Generating a Power-Fail Interrupt

Using the FM31xxx Power-Fail Comparator

Overview

The FM31xxx Integrated Processor Companion feature a general purpose comparator that can be used to generate an early power-fail warning. This warning signal can be used to drive a microcontroller interrupt input. It should occur before V_{DD} drops too low to provide the system with enough time to save critical data to nonvolatile RAM. It also provides a mechanism for polling the power condition to prevent conducting critical activity during a brownout condition.

Power Supply Monitoring

An early power-fail warning can be generated using the FM31xxx on-board comparator and used as a system interrupt for a host microcontroller. This application note shows two implementations using the comparator. In a typical system, the comparator's output is tied to the NMI input (non-maskable interrupt) of a microcontroller.

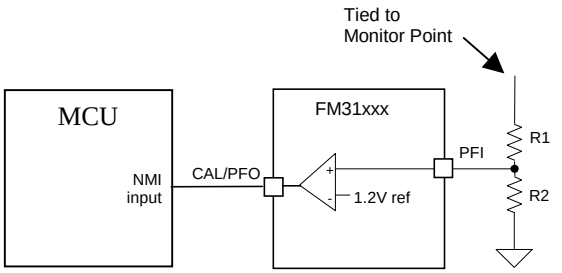

Figure 1. System Hookup & Monitor Point

The comparator provides a single input for monitoring voltage. The other comparator input is tied to an on-board 1.2V precision reference. Since the comparator is non-inverting, the output will drive to a low state when the PFI input drops below 1.2V. To use this function as a power-fail interrupt, the PFI input should be connected via a voltage divider to a power supply voltage.

First Method: AC line-operated systems use voltage-regulated power to provide a stable voltage to guarantee circuit operation. An unregulated power supply always precedes the regulator. As the unregulated voltage varies, the regulated voltage remains stable – to a point. As the unregulated supply voltage drops, due to a failure or normal system shutdown, the processor and memory subsystem is better served by knowing that power is lost well before the regulator drops out. An early warning mechanism can be provided to the processor host of this impending power loss. A non-maskable interrupt (NMI) is a means by which the host can prepare for this soon-to-be loss of power. The unregulated side within the power supply can be monitored. In this case, the unregulated input voltage will begin to drop before the regulated output V_{DD} is affected. A common line-operated power supply that is well suited to this type of application is shown in Figure 2a.

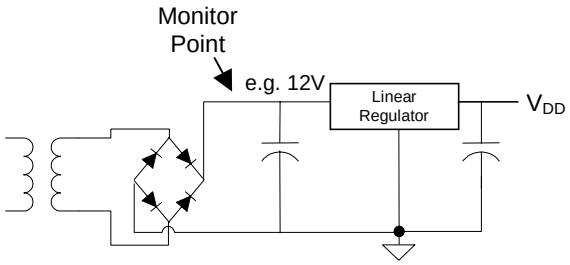

Figure 2a. Line-Operated Power Supply

Second Method: A regulated LDO output (V_{DD}) can be monitored for a drop below a selected threshold so that the interrupt occurs at a higher voltage than the processor reset trip point. A typical battery-based power supply that is suited to this approach is shown in Figure 2b.

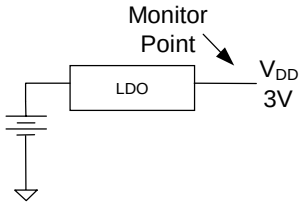

Figure 2b. Battery-Based Power Supply

In the first case, the interrupt is generated in response to a voltage drop on the regulator's unregulated side, in this example, 12V. This will occur well before the regulated output V_{DD} drops. In the second case, the power supply is a primary battery and LDO (low dropout) regulator. The LDO output may begin to drop soon after the battery voltage falls, so it is most accurate to monitor V_{DD} directly. Most LDO regulators exhibit a linear relationship between V_{IN} and V_{OUT} when V_{IN} drops below V_{OUT}.

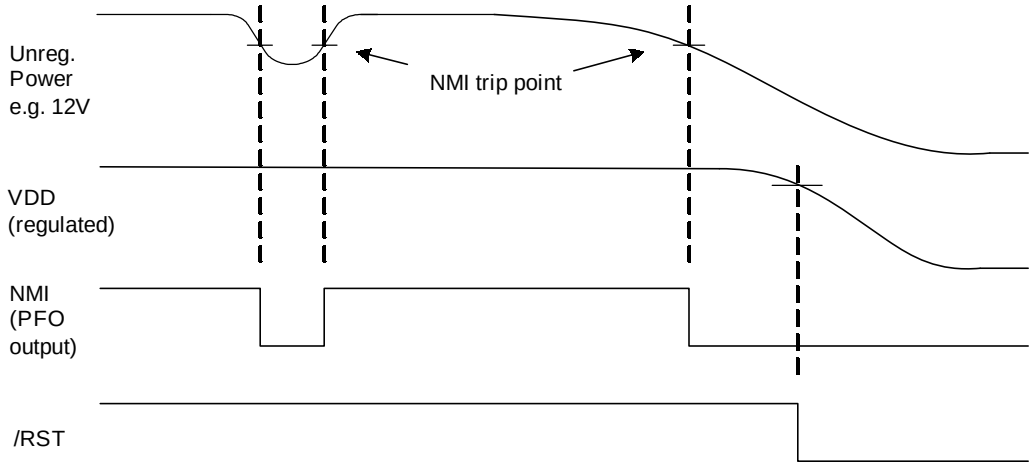

Figure 3a. Power Down Events for Line-Operated Supply

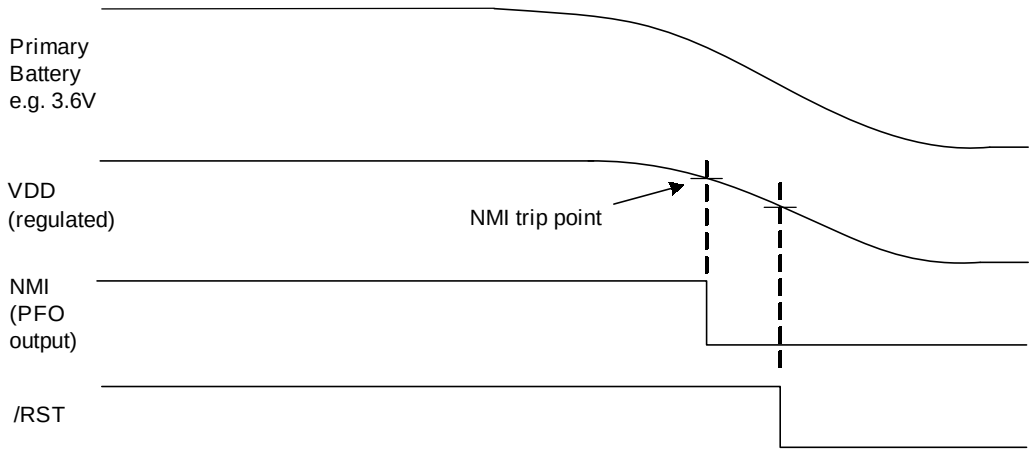

Figure 3b. Power Down Events for Battery Supply

The early power-fail comparator can support either approach, but the first case provides a warning much earlier. In the case of monitoring an unregulated power supply, power loss due to a brownout condition and complete power down are shown in Figure 3a. An interrupt is generated well before V_{DD} drops since the monitored voltage occurs at an earlier point in the power supply. In the case of a primary battery, V_{DD} is directly monitored and there is no brownout case.

In order to trigger the NMI as shown in Figure 3, the NMI trip point must be carefully chosen. The goal is to generate an NMI signal as soon as possible when power drops, but not generate an NMI within the normal tolerance or ripple of the power supply, yet not so late that the voltage regulator starts to drop out.

Example: a 12V power supply with a ± 10% tolerance is allowed a 10.8V output level, so the PFO pin should be set to trip no higher than 10.3V, if you provide an additional 0.5V margin. A lower limit on the supply trip point is the minimum V_{IN} specification for the linear regulator. A low dropout regulator requires very little headroom whereas a conventional linear regulator needs more input voltage. For example, a 5V linear regulator may have a dropout specification of 2V, meaning that V_{OUT}, or system V_{DD}, will begin to drop when the input voltage reaches 7V. Therefore in this example, the PFO trip point should be set between 10.3V and 7V.

The power supply sense circuit is a simple voltage divider, tied to the unregulated supply, and the tap point applied to an on-chip comparator, the PFI pin. The resistor values are chosen to generate an NMI when the divided voltage on the PFI input goes below the 1.2V comparator reference. The trip point is defined by a simple resistor divider ratio. NOTE: Be sure the PFI pin does not exceed V_{DD} (min), or 4.5V.

The equation is:

$$V_{TRIP} \times \frac{R2}{R1+R2} = 1.2V$$

For example, if the power supply is 12V ± 10% and the regulated output V_{DD} is 5V ± 10%. And if the desired NMI trip point V_{TRIP} is 9V, then the divider ratio R2/(R1+R2) is 0.133. Note: Resistors R1 and R2 are labeled in Figure 1.

The easiest solution is to choose one resistor then solve for the other.

$$\text{We know, } 0.133 = \frac{R2}{R1+R2}$$

$$\text{And, } R1+R2 = \frac{R2}{0.133}$$

$$\text{So, } R1 = \frac{R2}{0.133} - R2$$

For R2=47K, R1 = 306K.

Additional Considerations

The slew rate of the power supply on the unregulated side can dictate the amount of time that is available for backing up data after an NMI occurs and before a reset occurs. For example, assume the nominal 12V supply has a slew rate of 0.5 V/ms. For this example, an NMI is generated at 9V, and the 5V linear regulator begins to drop out at 7V. The NMI will occur 1ms before the regulator drops out and the FM31xxx power V_{DD} begins to drop.

The comparator is a convenient way to generate an interrupt which provides enough time for a processor to save critical data to nonvolatile RAM. It can also be used to poll the power conditions. Once the NMI occurs, it is advisable to monitor the signal continuously and to avoid conducting critical activity until the NMI clears. If the NMI is the result of a brown out, then eventually the condition will clear and normal operation can resume. If it is not a brown out, the reset /RST will eventually be asserted.