wavefront SEMICONDUCTOR

AL3101/2CG

DSP-1K(M/S) Audio Processors

Lead free – Complies with RoHS directive

DSP-1K(M/S) Audio Processors AL3101/2CG

General Description

The DSP-1K Audio Processor is a fast, low cost signal processor optimized for signal filtering, equalization, and dynamics processing. Large word size provides easy, accurate algorithm creation for audio and other high dynamic range applications.

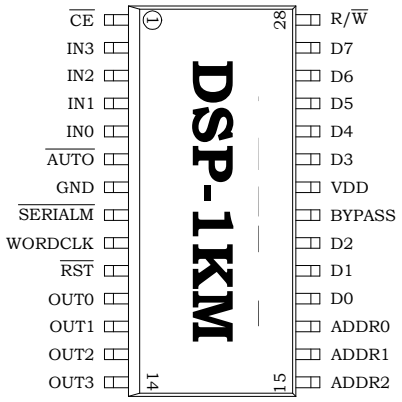
The DSP-1KM (AL3101CG) supports three control interface methods: serial or parallel with a host microprocessor, or stand-alone autoloading from a serial PROM. The DSP-1KS (AL3102CG) supports the serial microprocessor interface.

Features

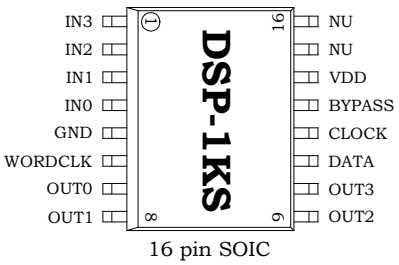
- High-Speed, low-cost audio DSP engine
- Internal PLL - User need only supply WORDCLK at the desired sample rate.
- 1024 instructions per WORDCLOCK. (49.152 MIPS @ 48kHz.)
- Single cycle instruction execution
- Log and anti-log instructions
- Single cycle calculate and move
- Internal Instruction and Data RAM
- 4 stereo inputs and outputs
- Peak meters on all inputs and outputs
- Parallel and serial microprocessor interface
- Stand alone operation with serial PROM.
- Lead free – complies with RoHs directive.

Not recommended for 5V designs.

Applications	Functions					
Products	**EQ**	**Dynamics**	**Effects**	**Mixing/Routing**	**Crossover**	**Psychoacoustic**
Mixers	√	√		√		
Outboard	√	√	√	√		√
Stomp boxes	√	√	√			
Guitar Amps		√	√			
Synthesizers			√	√		
Karaoke	√	√	√	√		√
Active Speakers	√				√	√
DJ	√	√	√	√		



28 pin SOIC
300 mils wide



16 pin SOIC
300 mils wide

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Pin Descriptions

DSP-1KM AL3101CG 28-Pin Package

(* Pullup to V_{DD} via nominal 30kΩ resistor. ⁺ Pulldown to Gnd via nominal 30kΩ resistor.)

Pin#	Name	Pin Type	Description
1	$\overline{CE}$	In*	Active low chip enable. 1: Disabled, 0: Enabled.
2	IN3	In	ADC Input serial channels 6&7.
3	IN2	In	ADC Input serial channels 4&5.
4	IN1	In	ADC Input serial channels 2&3.
5	IN0	In	ADC Input serial channels 0&1.
6	$\overline{AUTO}$	In*	Active low autoload select. 1: Enable microprocessor interface, 0: Load code from external serial PROM.
7	GND	Ground	Ground connection.
8	$\overline{SERIALM}$	In*	Active low serial microprocessor interface select. 1: Enable parallel interface or PROM, 0: Enable serial interface.
9	WORDCLK	In	Wordclock input, used by PLL to derive other signals.
10	$\overline{RST}$	In*	Active low reset.
11	OUT0	Out	DAC Output serial channels 0&1.
12	OUT1	Out	DAC Output serial channels 2&3.
13	OUT2	Out	DAC Output serial channels 4&5.
14	OUT3	Out	DAC Output serial channels 6&7.
15	ADDR2	In*	Address bit 2.
16	ADDR1	In*	Address bit 1.
17	ADDR0	In*	Address bit 0.
18	D0	I/O*	Data I/O 0 (Data line in serial microprocessor mode).
19	D1	I/O⁺	Data I/O 1 (Clock line in serial microprocessor mode).
20	D2	I/O*	Data I/O 2
21	BYPASS	I/O	Connect to V_{DD} power pin.
22	VDD	Power	V_{DD} power pin.
23	D3	I/O*	Data I/O 3.
24	D4	I/O*	Data I/O 4.
25	D5	I/O*	Data I/O 5.
26	D6	I/O*	Data I/O 6.
27	D7	I/O*	Data I/O 7.
28	R/$\overline{W}$	In*	Read/Write select. 0: Read mode, 2: Write mode.

DSP-1KS AL3102CG 16-Pin Package

(* Pullup to V_{DD} via nominal 30kΩ resistor. ⁺ Pulldown to Gnd via nominal 30kΩ resistor.)

Pin#	Name	Pin Type	Description
1	IN3	In	ADC Input serial channels 6&7.
2	IN2	In	ADC Input serial channels 4&5.
3	IN1	In	ADC Input serial channels 2&3.
4	IN0	In	ADC Input serial channels 0&1.
5	GND	Ground	Ground connection.
6	WORDCLK	In	Wordclock input, used by PLL to derive other signals.
7	OUT0	Out	DAC Output serial channels 0&1.
8	OUT1	Out	DAC Output serial channels 2&3.
9	OUT2	Out	DAC Output serial channels 4&5.
10	OUT3	Out	DAC Output serial channels 6&7.
11	DATA	I/O*	Serial microprocessor interface data line.
12	CLOCK	In⁺	Serial microprocessor interface clock line.
13	BYPASS	I/O	Connect to V_{DD} power pin.
14	VDD	Power	V_{DD} power pin.
15	NC	None	No internal connection. For future compatibility, do not connect.
16	NC	None	No internal connection. For future compatibility, do not connect.

Electrical Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
Recommended Operating Conditions						
V_{DD}	Supply Voltage		3.15	3.3	3.45	V
I_{DD}	Supply Current	Note 1		31		mA
GND	Ground			0		V
Fs	Sample rate		30	48	50	kHz
Temp	Temperature		0	25	70	°C
Inputs ($\overline{AUTO}$, $\overline{SERIALM}$, ADDR2-0, D7-2, D0) - Internal 30kΩ pullup resistor.						
V_{IH}	Logical "1" input voltage		2.4	.	VDD	V
V_{IL}	Logical "0" input voltage		GND	.	0.8	V
V_T	Logic threshold			1.6		V
I_{IH}	Logical "1" input current				2	µA
I_{IL}	Logical "0" input current			110	220	µA
Inputs (CE, $\overline{RST}$, R/$\overline{W}$) - Schmitt trigger inputs with internal 30kΩ pullup resistor.						
V_{IH}	Logical "1" input voltage		2.5	.	VDD	V
V_{IL}	Logical "0" input voltage		GND	.	0.5	V
V_{TR}	Rising logic threshold			2.0		V
V_{TF}	Falling logic threshold			1.0		V
I_{IH}	Logical "1" input current				2	µA
I_{IL}	Logical "0" input current			110	220	µA
Inputs (D1) - Internal 30kΩ pulldown resistor.						
V_{IH}	Logical "1" input voltage		2.4	.	VDD	V
V_{IL}	Logical "0" input voltage		GND	.	0.5	V
V_T	Logic threshold			1.6		V
I_{IH}	Logical "1" input current				220	µA
I_{IL}	Logical "0" input current				2	µA
Inputs (IN3 - 0)						
V_{IH}	Logical "1" input voltage		2.4	.	VDD	V
V_{IL}	Logical "0" input voltage		GND	.	0.8	V
V_T	Logic threshold			1.6		V
I_{IH}	Logical "1" input current				2	µA
I_{IL}	Logical "0" input current				2	µA
Inputs (WORDCLK) - Schmitt trigger input						
V_{IH}	Logical "1" input voltage		2.5	.	VDD	V
V_{IL}	Logical "0" input voltage		GND	.	0.5	V
V_{TR}	Rising logic threshold			2.0		V
V_{TF}	Falling logic threshold			1.0		V
I_{IH}	Logical "1" input current				2	µA
I_{IL}	Logical "0" input current				2	µA
Outputs (OUT3-0, D7-0)						
V_{OH}	Logical "1" output voltage	Unloaded		VDD		V
V_{OL}	Logical "0" output voltage	Unloaded		GND		V
I_{OH}	Logical "1" output current		-6.0			mA
I_{OL}	Logical "0" output current		6.0			mA

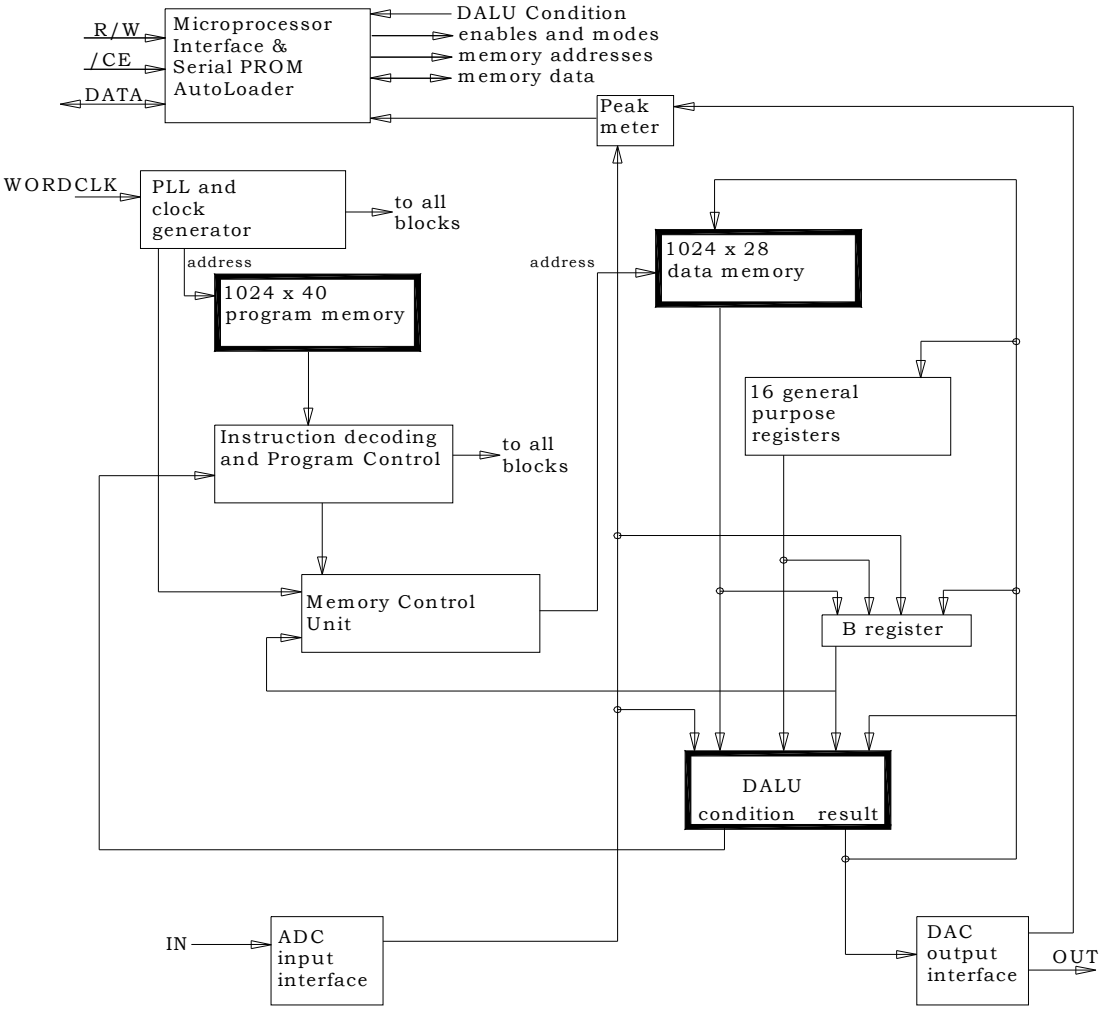
Note 1: Tested using AN3101-06.ASM which uses the AL3101CG to its fullest.

Architecture Overview

The DSP-1K contains the following major blocks:

- Data/arithmetic/logic unit (DALU)
- 1024 x 40-bit Instruction RAM
- 1024 x 28-bit Data RAM (Sample RAM)
- 16 x 28-bit General Purpose Registers (Direct Address Memory, Scratchpad RAM)
- Memory control unit
- ADC input interface
- DAC output interface
- Instruction decoding and program control unit
- Microprocessor interface
- PLL and clock generator
- Serial PROM auto-loader
- Peak-metering unit

Architecture Block Diagram



Architecture Details

Notation

The DSP-1K stores and operates on data using a fixed-point, two's complement number in a sign-integer-fraction format, written as S3.X. The S signifies the sign bit, the 3 signifies the number of integer bits, the period signifies the binary point, and the X signify the number of fractional bits, which may be 24, 18, or 8.

Hexadecimal numbers throughout this document are indicated by the prefix "$". The acronym MSB stands for Most Significant Bit, and LSB is Least Significant Bit, indicating bits on the leftmost or rightmost of the value respectively.

Data/Arithmetic/Logic Unit

The DALU performs all the arithmetic and logical operations on the data in the DSP-1K. All instructions are executed in one clock cycle. In general, the DALU uses a 28-bit-wide datapath; however the exact width depends on the instruction being executed. If the instruction uses less than the number of available bits, then the MSBs are used. If the instruction needs more than the number of available bits, then the number is padded with zeroes in its LSBs. The DALU consists of:

- A 28-bit x 22-bit multiplier producing a 28-bit result. The 28-bit number is in a S3.24 format and the 22-bit number is in a S3.18 format.
- A 28-bit accumulator (A) in S3.24 format
- A 28-bit register (B) in S3.24 format that the accumulator may be copied to
- 16 28-bit General Purpose Registers in S3.24 format
- ADC input registers
- DAC output registers

Instruction RAM

The Instruction RAM consists of 1024 address locations continuously cycled through on every wordclock period, starting with instruction 0 at the beginning of the period and completing the execution of instruction 1023 by the end. This is synchronized with the ADC Inputs and DAC Outputs such that a new sample is received after the execution of instruction 1023 and before instruction 0. This type of cycling is advantageous for processing streaming data such as audio, where the same program is applied to each sample as it is received.

For a detailed description of the instructions and their usage, please refer to the DSP-1K Assembly Language Manual IM3101-02 in the Development System software package. For the instructions executing in the Instruction RAM, the internal program memory map is explained in the following table.

Internal Program Memory Map

Address	Description
$000-$3FF	Data RAM
$400-$40F	General Purpose Registers
$410-$417	Serial I/O
$418	LOG16 field extract – READ ONLY
$419	ADC Input pins – READ ONLY
$41B	Null output – WRITE ONLY
$421-$42F	DAC Output pins – WRITE ONLY

For the parallel microprocessor interface, the Instruction RAM is selected by the RAM Select bits, bits 3-2 of the Target Address MSB. For the serial microprocessor interface, the Instruction RAM is memory mapped to addresses $0-$3FF. Microprocessor accesses complete at the next instruction clock, and do not usurp the Instruction RAM address and data busses.

Data RAM

The Data RAM consists of 1024 storage locations, and stores values in S3.24 format. It is mapped in the range of $0-$3FF of the internal memory map, and the range of $800-$BFF of the serial microprocessor interface memory map. For the parallel microprocessor interface, the Data RAM is selected by the RAM Select bits, bits 3-2 of the Target Address MSB. Accessing the Data RAM with a microprocessor may usurp the Data RAM address and data bus during an internal program access. To avoid access collision, use the Last Data Access Mode (Target MSB bit 5 for parallel microprocessor interface, Control Word 1 bit 7 for serial microprocessor interface).

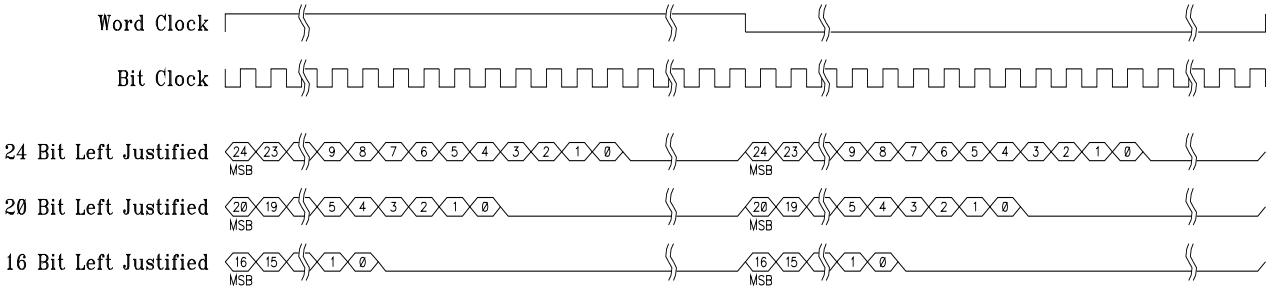
Memory Control Unit

To automatically implement circular addressing, the effective address of a Data RAM memory location is calculated by adding the address portion of the instruction to a counter which decrements once per sample period. (This offset is not added to the addresses which access the ADC Input, DAC Output or the 16 General Purpose Registers.) This counter is synchronized with the ADC Inputs, DAC Outputs and the program counter such that the decrement occurs after the execution of instruction 1023 and before the execution of instruction 0. As the value of the offset counter cannot be accessed, the exact physical address where values are stored cannot be determined (only the relative addresses used in the program are effective in accessing determinate locations), therefore if the microprocessor and the internal program wishes to exchange data through the microprocessor interface, the General Purpose Registers should be used. This feature may be turned off if desired by Control Word 1 bit 1 of the Microprocessor Interface.

ADC Input Interface

The ADC input bitclock rate is 64 times the WORDCLK frequency, internally generated by the PLL, reading in 16, 20, or 24 bit of data from the start of each frame depending on the setting of bits 1-0 in Control Word 0.

ADC Format Timing



The data is read into the 24 LSBs of the 28-bit internal datapath and sign-extended into the upper bits to create a 28-bit number, resulting in the ADC having an effective range of +0.5 to -0.5.

> For example, a full scale negative 24-bit ADC input of $800000 would become $F800000, which in the S3.24 format is equivalent to -0.5.

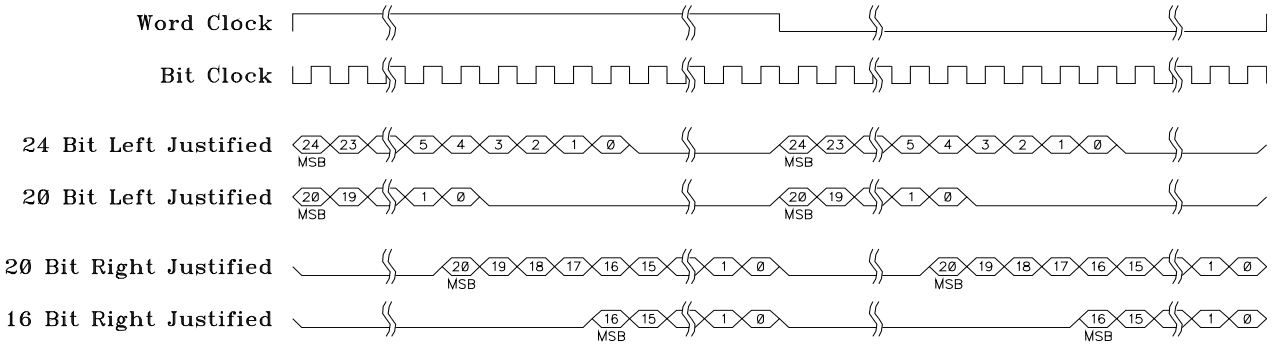
For the internal program, the ADC Inputs are read from addresses $410-$417. Though these addresses are the same as for the DAC Outputs, they are separate registers and will not read from the DAC Output registers.

It is also possible to directly read the input IN[3:0] (pins 2-5). Reading address $419 will read IN[3:0] into bits 23-20 (just below the binary point). This will override the Serial Input Enable muting in Control Word 0, and allows the use of these pins as flags within a program.

DAC Output Interface

The DAC output bitclock rate is 64 times the WORDCLK frequency, internally generated by the PLL, outputting 16, 20, or 24 bit of data in each frame depending on the setting of bits 1-0 in Control Word 0.

DAC Format Timing



The outputs are taken as the 24 LSBs of the number written to them, which aligns the DAC output value with the ADC input value in the location of their binary points.

> For example, $F800000 in the S3.24 format, which is equivalent to -0.5, would become $800000, a full scale negative 24-bit ADC input.

The MSBs are checked to verify that they are all the same as the sign bit. If not, prior to being written to the DAC register, the value is saturation limited to the maximum negative or positive value based on the sign bit. For the internal program, DAC outputs are written to addresses $410-$417. Though these addresses are the same as for the ADC, they are separate registers and will not overwrite the ADC values.

It is also possible to directly drive the serial output pins OUT[3:0]. By writing to the internal memory map address range $421-$42F, the Serial OUTn Enables muting in Control Word 0 are overridden, and bits 23-20 of the data can be placed on the pins. Which pins are written to are controlled by the 4 LSBs of the address. Once a pin is directly written to, it will stay in this direct write mode until it is written to as a serial output by writing to the range $410-$417.

DAC Direct Output Write Addresses

Address	Outputs	Bits Set
$421	OUT0	20
$422	OUT1	21
$423	OUT1, OUT0	21, 20
$424	OUT2	22
$425	OUT2, OUT0	22, 20
$426	OUT2, OUT1	22, 21
$427	OUT2, OUT1, OUT0	22, 21, 20
$428	OUT3	23
$429	OUT3, OUT0	23, 20
$42A	OUT3, OUT1	23, 21
$42B	OUT3, OUT1, OUT0	23, 21, 20
$42C	OUT3, OUT2	23, 22
$42D	OUT3, OUT2, OUT0	23, 22, 20
$42E	OUT3, OUT2, OUT1	23, 22, 21
$42F	OUT3, OUT2, OUT1, OUT0	23, 22, 21, 20

For example, if bit 0 of the address is set (address $421), OUT0 will reflect the data from bit 20, the remaining outputs will operate in the normal serial output mode. And if bits 1 and 2 of the address are set (address $426), OUT1 will reflect data from bit 21 and OUT2 will reflect data from bit 22, while OUT0 and OUT3 will continue to operate in their current mode.

Microprocessor Interface

The DSP-1K allows read and write access to the internal Instruction RAM, Data RAM, and General Purpose Registers. In addition, there are Peak Meters on all 8 input and output channels which may be read, Control Words which may be written to, and a Status Word which may be read. Selection of the data to be read or written is done through a combination of address and settings in the Control Words.

There are three interface formats available on the DSP-1KM depending on the states of /AUTO (pin 6) and /SERIALM (pin 8), as shown on the table below, and the interface may be switched on the fly as long as the selection pins never go through the reserved state. The DSP-1KS only supports the serial microprocessor interface.

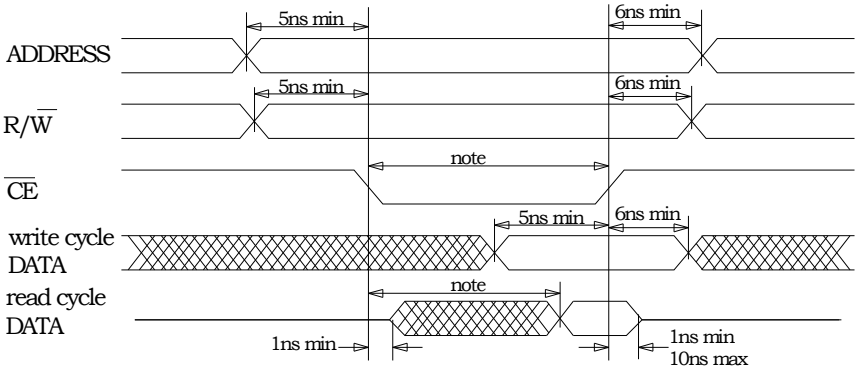
Interface Selection

Function	$\overline{\text{AUTO}}$ (Pin 6)	$\overline{\text{SERIALM}}$ (Pin 8)
Reserved	0	0
Serial PROM Autoload Interface	0	1
Serial Microprocessor Interface	1	0
Parallel Microprocessor Interface	1	1

Parallel Microprocessor Interface (DSP-1KM Only)

The parallel microprocessor interface uses a conventional 8-bit microprocessor interface. The R/W pin and address pins must be set up before the CE pin pulses low, and they must be held until after CE rises high again. During writes (R/W low), the data must be stable around the rising edge of CE. During reads, data becomes stable shortly after CE falls and remains valid until shortly after CE rises.

Parallel Microprocessor Interface Access Timing



note:
CE width min =
read cycle DATA valid after CE falls max =
$\left(\frac{\text{WORDCLK cycle}}{1024} + 32\text{ ns}\right)$
(52ns with 48 kHz WORDCLK)

Parallel Microprocessor Read Addresses

A[2:0] (Pins 15-17)	Description
111	Status Word
110	Reserved
101	Reserved
100	Data MSB
011	Data
010	Data
001	Data
000	Data LSB

Parallel Microprocessor Write Addresses

A[2:0] (Pins 15-17)	Description
111	Control Words
110	Target Address MSB*
101	Target Address LSB
100	Data MSB
011	Data
010	Data
001	Data
000	Data LSB

*Note: See Target Address MSB table for details.

All Data are LSB aligned. Thus when reading locations with fewer than 40 bits, upper Data bits are unused and are read as zeroes. When the Target Address MSB is written to address 6, the data written to addresses 4-0 is written to the target address.

***Target Address MSB**

Bit #	Description	
7:6	Reserved, set to 1.	
5	Last Data Access Mode: 1: Execute access immediately, 0: Access during instruction 1023. +	
4	Read/Write Select. 1: Execute read, 0: Execute write.	
3:2	**RAM Select[1:0]**	**Description**
	11	General Purpose Registers
	10	Data RAM
	01	Reserved
	00	Instruction RAM
1:0	Target Address [9:8].	

+Note: An immediate access to Data RAM can corrupt the memory if the DSP-1K is executing a memory access at the same time. The safest way to do this is to set this bit to 0 and not access memory on instruction 1023. If immediate access is required, then the external device accessing the DSP-1K should monitor the WORDCLK signal and determine if the instruction being executed is safe for memory access. Writes (but not reads) to General Purpose Registers are also subject to this restriction.

To read from the RAMs or the General Purpose Registers, Control Word 1 bit 5 needs to be set to 1 along with the RAM Select bits. Writes may be done independent of the setting of that bit.

Parallel Microprocessor Interface Control Words

Both Control Words are at address 7. Bit 7 indicates which Control Word is being written.

Parallel Microprocessor Interface Control Word 0

Bit #	Description	
7	Control Word Select. 0: Select Control Word 0.	
6:3	Serial OUT[3:0] Enable. 1: Enable OUTn; 0: Mute OUTn. Resets to 0.	
2	Serial Input Enable. 1: Enable serial inputs ; 0: Mute serial inputs. Resets to 0.	
1:0	**ADC/DAC Mode Select[1:0]** Resets to 00.	**Description**
	11	24 bit, ADC/DAC left justified
	10	20 bit, ADC/DAC left justified
	01	20 bit, ADC left justified, DAC right justified
	00	16 bit, ADC left justified, DAC right justified

Parallel Microprocessor Interface Control Word 1

Bit #	Description
7	Control Word Select. 1: Select Control Word 1.
6	Memory Write Disable. 1: Disable writing to memory under program control; 0: Enable writing to memory. Resets to 1.
5	Read Select. 1: Read Status Word or RAMs; 0: Read Peak Meters. Resets to 0.
4	Peak Meter Select. 1: Read output meters; 0: Read input meters. Resets to 0.
3	Wordclock Phase. 1: Invert wordclock; 0: Normal wordclock. Resets to 0.
2	MAC Rounding. 1: Round MAC results; 0: Truncate MAC results. Resets to 0.
1	Memory Offset Counter. 1: Disable memory offset counter; 0: Enable counter. Resets to 1. *
0	Reserved, set to 0.

*Note: A down counter which is added to Data RAM addresses. See Memory Control Unit for details.

Status Word

The Status Word is read from address 7 of the parallel microprocessor interface, and indicates the status of several settings with a 1 if true.

Status Word

Bit #	Description
7	DAC Output Overflow. Output clipped.
6	MAC Overflow. Clipped to ±8.0 on non-integer instructions.
5:2	OUT[3:0] Muted.
1	Inputs Muted.
0	Memory Access Complete.

Peak Meters

To read ADC Input Peak Meter registers, set Control Word 1 bits 5-4 to 00. To read DAC Output Peak Meter registers, set Control Word 1 bits 5-4 to 01.

Input Peak Meter Read Addresses

A[2:0] (Pins 15-17)	Description
111	Channel 7 Peak Meter.
110	Channel 6 Peak Meter.
101	Channel 5 Peak Meter.
100	Channel 4 Peak Meter.
011	Channel 3 Peak Meter.
010	Channel 2 Peak Meter.
001	Channel 1 Peak Meter.
000	Channel 0 Peak Meter.

Output Peak Meter Read Addresses

A[2:0] (Pins 15-17)	Description
111	Channel 7 Peak Meter.
110	Channel 6 Peak Meter.
101	Channel 5 Peak Meter.
100	Channel 4 Peak Meter.
011	Channel 3 Peak Meter.
010	Channel 2 Peak Meter.
001	Channel 1 Peak Meter.
000	Channel 0 Peak Meter.

Serial Microprocessor Interface (DSP-1KM and DSP-1KS)

The host microprocessor communicates to the DSP-1K in a special serial format. To select this interface, set AUTO (pin 6) high and SERIALM (pin 8) low. The DSP-1KS uses this access method only.

Serial Microprocessor Interface Format and Access Timing

The basic format for the micro serial interface is:

Attn Sel R/W A7 A6 A5 A4 A3 A2 A1 A0 DN DN-1 DN-2 … D2 D1 D0 Attn Desel

⇑ ⇑ Write mode only

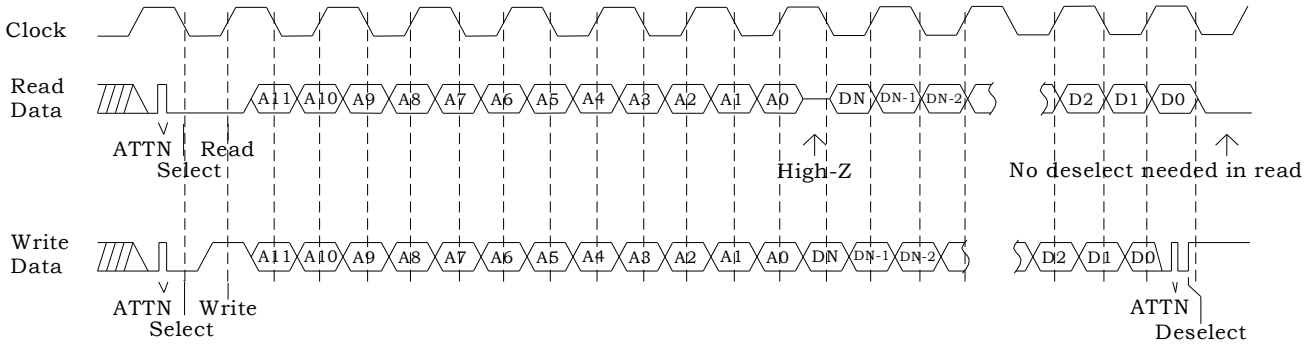
Attn: A 0-1-0 is used to signal attention/start.
Sel/Desel: 0:Select; 1:Deselect.
R/W: 0:Read; 1:Write
A7 - A0:Address
DN - D0: Data

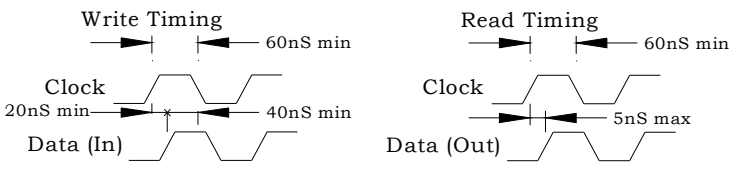
Note 1: There is a period of High-Z during a read between A0 and the first data bit shifted out. This must be at least 6 instruction clocks long (123ns for 48kHz sample rate), or until after instruction 1023 if in Last Data Access Mode.

Note 2: As long as data is being sent during a write, the address will be automatically incremented. Therefore only a start address need be sent.

Note 3: Clock only the number of data bits needed for the particular memory accessed.

Note 4: The phase of the clock is unimportant.





Serial Microprocessor Read Addresses

Address	Description
$000–$3FF	Instruction RAM
$407	Status Word
$500–507	Input Peak Meters
$508–50F	Output Peak Meters
$800–BFF	Data RAM
$C00–C0F	General Purpose Registers

Serial Microprocessor Write Addresses

Address	Description
$000–$3FF	Instruction RAM
$400	Control Word 0
$401	Control Word 1
$800–$BFF	Data RAM
$C00–$C0F	General Purpose Registers

Serial Microprocessor Interface Control Words

Control Word 1 differs from the Parallel Microprocessor Interface the use of bit 7 to control the Last Data Access Mode. Bits 5-4, which control access to Peak Meters in the parallel interface, have no effect with the serial interface.

Serial Microprocessor Interface Control Word 0

Bit #	Description	
7	Reserved, set to 0.	
6:3	OUT[3:0] Enable. 1: Enable OUTn; 0: Mute OUTn. Resets to 0.	
2	Serial Input Enable. 1: Enable serial inputs ; 0: Mute serial inputs. Resets to 0.	
1:0	**ADC/DAC Mode Select** Resets to 00.	**Description**
	11	24 bit, ADC/DAC left justified
	10	20 bit, ADC/DAC left justified
	01	20 bit, ADC left justified, DAC right justified
	00	16 bit, ADC left justified, DAC right justified

Serial Microprocessor Interface Control Word 1

Bit #	Description
7	Last Data Access Mode: 1: Execute access immediately, 0: Execute access on instruction 1023. [+]
6	Memory Write Disable. 1: Disable writing to memory under program control; 0: Enable writing to memory. Resets to 1.
5:4	Reserved, set to 0.
3	Wordclock Phase. 1: Invert wordclock; 0: Normal wordclock. Resets to 0.
2	MAC Rounding. 1: Round MAC results; 0: Truncate MAC results. Resets to 0.
1	Memory Offset Counter. 1: Disable memory offset counter; 0: Enable counter. Resets to 1.
0	Reserved, set to 0.

[+] Note: An immediate access to Data RAM can corrupt the memory if the DSP-1K is executing a memory access at the same time. The safest way to do this is to set this bit to 0 and not access memory on instruction 1023. If immediate access is required, then the external device accessing the DSP-1K should monitor the WORDCLK signal and determine if the instruction being executed is safe for memory access. Writes (but not reads) to General Purpose Registers are also subject to this restriction. When using the Last Data Access Mode for reads, the microprocessor must pause after sending the last address bit clock until after instruction 1023 has executed. This delay may be achieved by waiting one full sample period, or waiting until the DSP-1K's internal wordclock rises.

Serial Microprocessor Interface Status Word and Peak Meters

The Serial Microprocessor Interface Status Word and Peak Meters are exactly the same as the Parallel Microprocessor Interface versions. Please refer to the relevant sections in the parallel interface section.

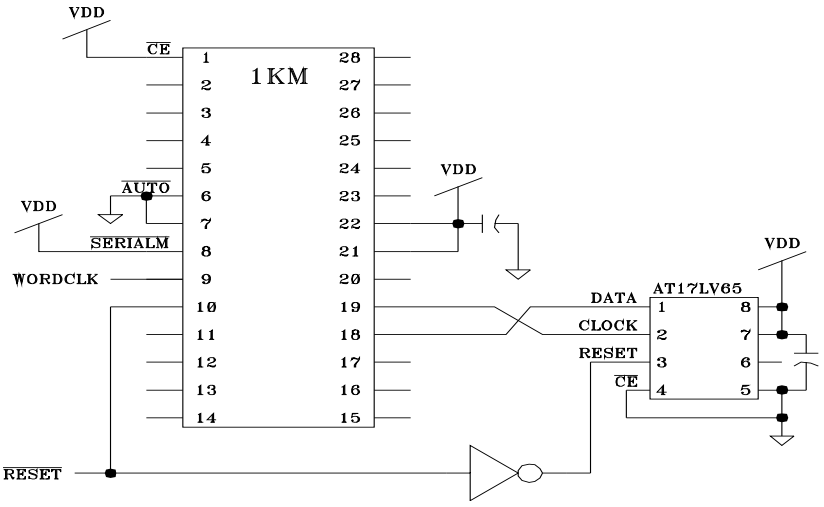
Serial PROM Autoload Interface (DSP-1KM only)

If /AUTO (pin 6) is low and /SERIALM (pin 8) is high at power on, the serial PROM autoload interface is enabled and the DSP-1KM will operate without a host microprocessor and load its program information from an external serial PROM through D1-D0 (pins 19-18). This method is not available in the DSP-1KS.

Program information and control words may be stored in a serial configuration EEPROM such as the ATMEL AT17LV65. A capacity of 1024 instruction words x 5 bytes/word + 2 control bytes = 5122 bytes, or 40976 bits, is required. The first bit from the EEPROM is the MSB of the first instruction (Instruction RAM address 0), the second bit is the second MSB of the first instruction word, the 41st bit from the EEPROM is the MSB of the second instruction of the DSP-1KM, and so forth. This pattern continues until 40960 bits are used, the 40960th bit being the LSB of the last word in the DSP-1KM's instruction memory. The next 8 bits fill Control Word 0, MSB first; the following 8 bits fill Control Word 1. Any other bits in the EEPROM are ignored.

The order of events during autoload is as follows: The /AUTO and /RST pins must be held low while power supplies stabilize; /SERIALM must be high. After circuits external to the DSP-1KM drive /RST high, the DSP-1KM waits 1024 WORDCLK periods for the PLL to stabilize. Then for each of the next 1024 WORDCLK periods, the DSP-1KM produces forty 160ns pulses spaced 160ns apart (320ns period) on D1 (pin 19). At each rising edge one bit is accepted on D0 (pin 18). The first forty pulses load instruction address 0, MSB first, the next forty instruction address 1, and so forth. Sixteen more pulses are produced, loading Control Word 0 and Control Word 1, both MSB first. The loaded program runs for 1024 WORDCLK periods with Serial I/O muted, then Serial I/O is unmuted (if the Control Words allow).

Serial PROM Autoload Interface Suggested Connections



Reset Unit

Besides the /RST pin on the DSP-1KM, the DSP-1Ks have Power-On Reset circuitry built-in. To utilize Power-On Reset, simply power down the chip for no less than 0.1ms, then power up the chip, taking care that signals to the chip are never higher than the current V_{DD} level. The Reset is active for less than 2ms, thus signals should not be applied until V_{DD} has been stable for 2ms.

PLL and Clock Generator

The built-in PLL generates all necessary clocks from WORDCLK. This minimizes the external component count and lowers interconnection bandwidth, reducing EMI.

Peak-Metering Unit

Each sample period the peak-metering unit tests the 16 MSBs of the ADC Inputs and DAC Outputs, and saves the highest peak absolute value since the last reading of the meter. The scale of the reading approximates a logarithm: 2 units per decibel with a maximum value of $FC. When a meter is read, it is automatically cleared so that new peak values can be accumulated.

The following table shows the relationship between the ADC/DAC absolute value and the peak meter result returned. Very small values deviate from a true log (as shown below), but above $000008 the log conformance is good.

Peak Meter Result of Absolute Value

|ADC/DAC Value|	Peak Meter Result
$000000	$00
$000001	$02
$000002	$04
$000003	$05
$000004	$07
$000005	$08
$000006	$09
$000007	$0B
$000008	$0C
.....	...
$000010	$18
.....	...
$6BFFFF	$F8
$75FFFF	$F9
$7FFE00	$FB
$7FFF00	$FC

The result $FC is a special value indicating that the value being read is the largest possible number that can be expressed in 16 bits. You may consider it an indication that the number in question is either clipped or on the verge of clipping.

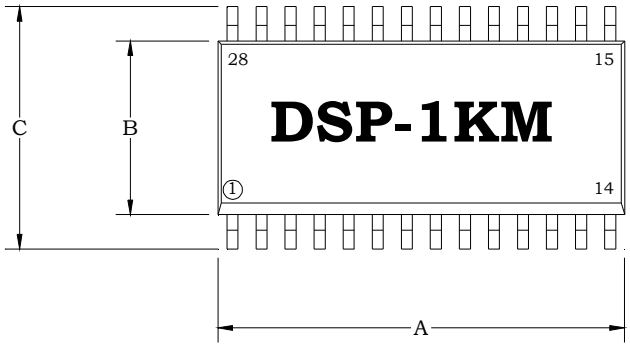
The peak meter circuit approximates absolute value by taking the one's-complement of negative numbers. From that absolute value, shifting and table lookup determine the reading. The following table illustrates the results for very small and very large inputs. In the range $000020 to $7FFEFF the peak meter reading is determined exactly by calculating the sum $24 + (12*S) + L. S is the number of bits that the leading one is further left than $000020 (for example, S is 5 for $000400), and L is the value from the table lookup, which is indexed by the 5 bits to the right of the leading one.

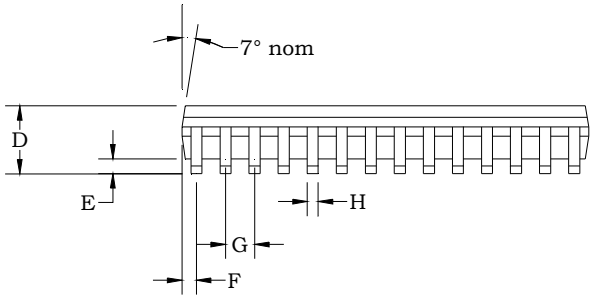
Lookup Table Results

Lower Limit	Upper Limit	Result L
00000	00001	$0
00010	00011	$1
00100	00101	$2
00110	00111	$3
01000	01010	$4
01011	01100	$5
01101	01111	$6
10000	10010	$7
10011	10101	$8
10110	11000	$9
11001	11011	$A
11100	11111	$B

Package Dimensions

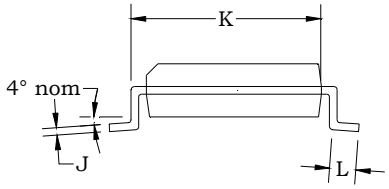
DSP-1KM AL3101CG 28-Pin Package



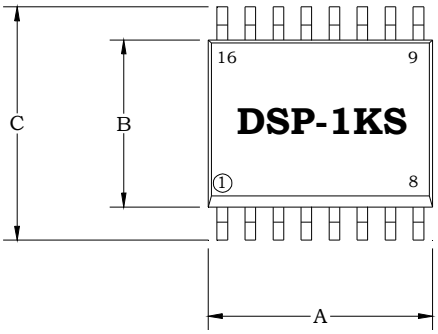


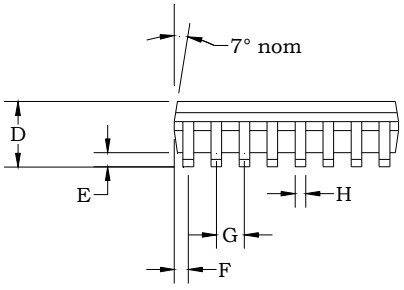
Dimensions (Typical)	Inches	Millimeters
A	0.705"	17.90
B	0.297"	7.54
C	0.406"	10.32
D	0.090"	2.28
E	0.008"	0.02
F	0.030"	0.76
G	0.050"	1.27
H	0.017"	0.40
J	0.011"	0.27
K	0.329"	8.33
L	0.033"	0.83

Note: Dimension “A” does not include mold flash, protrusions, or gate burrs.



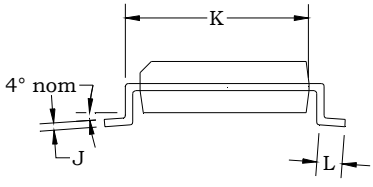
DSP-1KS AL3102CG 16-Pin Package





Dimensions (Typ)	Inches	Millimeters
A	0.402"	10.21
B	0.297"	7.54
C	0.406"	10.32
D	0.090"	2.28
E	0.008"	0.02
F	0.030"	0.76
G	0.050"	1.27
H	0.017"	0.40
J	0.011"	0.27
K	0.329"	8.33
L	0.033"	0.83

Note: Dimension “A” does not include mold flash, protrusions, or gate



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Application note revised September, 2006